

GRM6510 PRELIMINARY

Versatile GPS RF Front-End Receiver Module

The Rakon GRM6510 is a complete single conversion, Global Positioning System (GPS) miniature RF Front-End receiver module designed to receive the L1 C/A code signal at 1575.42 Mhz.

Product Description

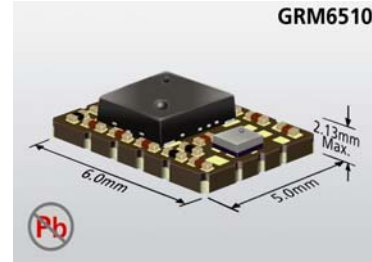
This entirely self-contained module incorporates an image rejection mixer, SAW filter and 0.5ppm TCXO. The module also has an impedance matched LNA input circuit with protected bias supply and feed components fitted for direct connection to an active antenna. It can also be connected to an LNA by making LNA2 active by SPI commands.

In the default mode, a 1bit or 2-bit (SGN, MAG) digital signal at a nominal IF frequency of 4 MHz, ready for subsequent digital processing, is provided at the output.

A wide range of reference frequencies are possible due to the fractional "N" PLL utilised, which gives the system designer significant flexibility in the choice of reference frequency. With a current consumption of only 19mA it represents a low power GPS receiver solution.

Under SPI control, many other outputs (such as serial streaming mode) and other operational configurations are available.

For optimum power management, the GRM6510 module includes power saving modes. It operates from 2.7V to 3.3V and over the temperature range of -30 to +80°C.



Features

- Complete, tested GPS L1 frequency receiver
- 6mm x 5mm x 1.95mm nominal ceramic package.
- 0.5ppm TCXO, LNA and SAW included.
- Impedance matched RF input for active antenna
- Antenna dc bias feed, short circuit protected
- Fully integrated Image reject mixer circuit.
- Interfaces easily between antenna and base bands by direct connection.
- Low power, fast standby mode.
- 2-bit Sign and Magnitude CMOS or differential IF signal or serial formats...
- Flexible options for the frequency reference and clock outputs.
- Reduces time to market as no receiver RF design time needed.
- Simplifies product BOM and purchasing requirements.
- Lead free, RoHS compliant module.

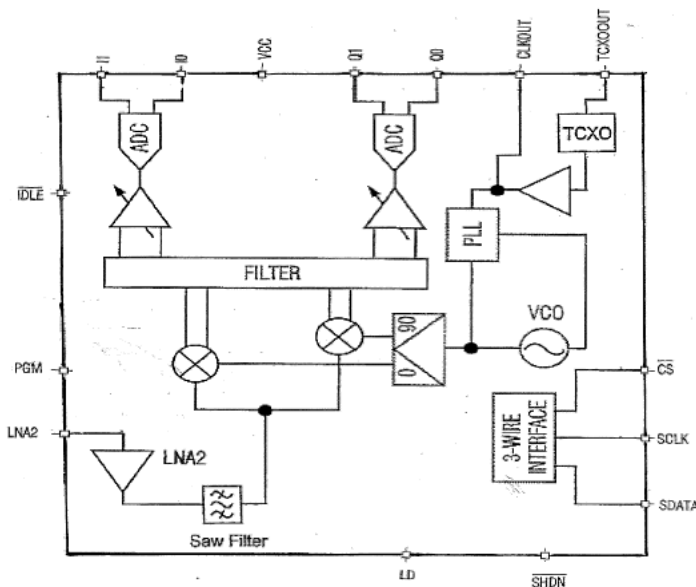


Figure 1. Block diagram



1.0 SPECIFICATION REFERENCES		
Parameter	Test Condition	
1.01	Model Series	GRM6510
1.02	RoHS Compliant	Yes

2.0 DC CHARACTERISTICS								
	Parameter	Condition		Minimum	Typical	Maximum	Units	Note
2.01	Supply Voltage	Analogue VCC		2.7	2.85	3.3	V	
2.02	Supply Current	Active	VCC		19		mA	VCC=2.85V
2.03		Idle mode	VCC		2.6		mA	TCXO and CLKOUT active
2.04		Shutdown	VCC		1.1		mA	Only TCXO active

3.0 RF and AC CHARACTERISTICS								
	Parameter	Condition		Minimum	Typical	Maximum	Units	Note
3.01	Cascaded Noise figure LNA_IN2	Active antenna bias load on LNA_IN2 or LNA2 enabled by SPI			5		dB	
3.02	Signal Bandwidth	-3dB points.			2.5		MHz	Other bandwidth options by SPI control
3.03	Input return loss LNA_IN2				10		dB	
3.04	Oscillator stability	-30 to 85°C.			0.5		ppm	

4.0 ANTENNA INTERFACES (Default mode) At typical value of VCC=2.85V								
	Parameter	Conditon		Minimum	Typical	Maximum	Units	Note
4.01	Voltage drop at LNA_IN2 from VCC	Sourcing 20mA at LNA_IN2			0.2V		V	
4.02	Short circuit protection current at LNA_IN2	LNA_IN2 is shorted to ground				57	mA	
4.03	Active antenna detection current at LNA_IN2	To assert logic high at ANTFLAG				1.1	mA	

5.0 Circuit description

The GRM6510 is a complete, easy to use, miniature single package GPS radio front-end that includes all critical elements such as LNA, SAW filter and RF input matching circuitry. It is designed to connect to an active antenna or LNA, and it typically provides IF data in either a 2-bit parallel format or serial format to the baseband. Other formats are available through SPI control for specialised applications.

The module provides a current limited (57mA limit) bias feed at LNA_IN2 which is sourced from VCC. This input has a good match to 50ohms to provide an ideal input for an active antenna or LNA. All bias feed components are fitted on the module. The LNA_IN2 is intended to be activated by either the bias current drawn by an active antenna, or it is turned on by SPI instruction (switching LNA2 on).

A SAW filter after the internal LNA provides protection against interfering signals and an image rejecting pair of mixers gives a typical 25dB rejection of the image. A fully integrated intermediate Frequency (IF) amplifier and filter stage follows. This filter has a nominal bandwidth of 2.5MHz and in the default state uses a 5th order response to give the best stop band attenuation.

The filtered IF signal is then amplified by an IF amplifier with AGC. Subsequently, an ADC converts the IF signal to a digital output. The AGC provides sufficient control range to ensure that the output signal level is held at an optimum level in the ADC. The 1bit or 2bit digital output (sign and magnitude) is suitable for direct interface to a baseband processor, or serial modes are available under SPI control.

A Rakon 0.5ppm TCXO provides the reference frequency for the internal PLL.

5.1 SPI control.

A highly versatile SPI control allows customisation of such parameters as: IF filter bandwidth, Filter center frequency, data quantisation (1-3 bits), output serial streaming, power control and frequency plan.

The serial interface is controlled by three signals: SCLK (serial clock), /CS (chip select), and SDATA (serial data). The control of the PLL, AGC, test and block selection is performed through the serial-interface bus from the controller. A 32-bit word, with the MSB (D27) being sent first, is clocked into a serial shift register when the chip-select signal is asserted low. The timing of the interface signals is shown in the figure 2 and table 5 below, along with typical values for setup and hold time requirements.

Figure 2. Timing diagram

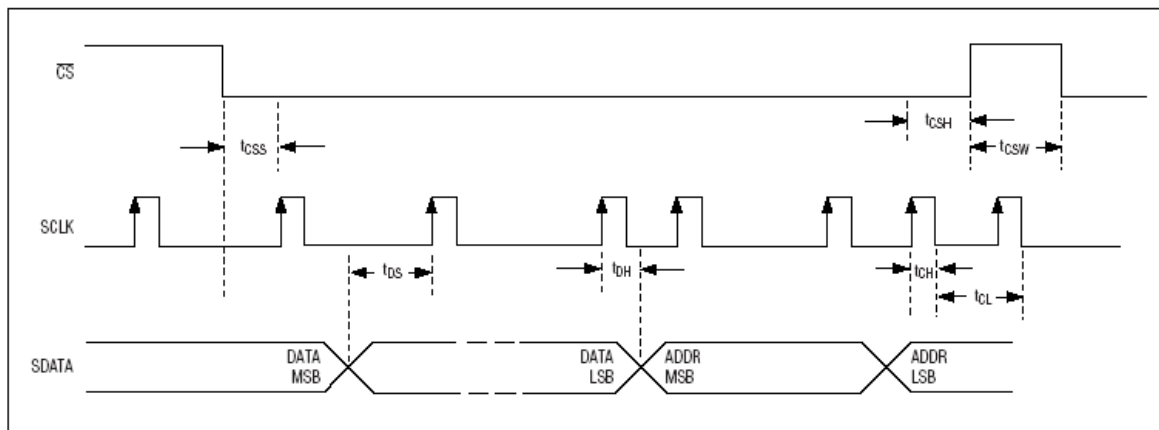




Table 5 Serial – Interface Timing Requirements			
SYMBOL	PARAMETER	TYPICAL VALUE	UNITS
tCSS	Falling edge of /CS to rising edge of the first SCLK time	10	ns
tDS	Data to serial-clock setup time	10	ns
tDH	Data to clock hold time	10	ns
tCH	Serial clock pulse-width high.	25	Ns
tCL	Clock pulse-width low	25	ns
tCSH	Last SCLK rising edge to rising edge of /CS	10	ns
tCSW	/CS high pulse width.	1	clock

5.2 Frequency plans

The GRM6510 is able to be fitted with various reference frequencies leading to different frequency plans. A reference frequency of either 16.367MHz or 16.368MHz (or others in this range) are directly compatible with many existing base-band processors and therefore is an ideal choice for applications where the GRM6510 can substitute a previous generation front end, giving significant space savings and easy integration.

Table 6 Supported frequency plans for default modes						
Device	Nominal Ref. frequency	Nominal IF frequency	Parallel Data output format	Reference frequencies selection		
				CLK	DATA	CS_
GRM6510	16.367MHz	4.188 MHz	2bit CMOS	0	1	0
	16.367667MHz	4.124MHz	2bit CMOS	0	1	0
	16.368MHz	4.092MHz	2bit CMOS	0	1	0
	32.768MHz	4.092MHz	2bit CMOS	0	1	1
	19.2MHz	4.092MHz	2bit CMOS	1	0	0
	18.414MHz	1.023MHz	2bit CMOS	1	0	1
	16.368MHz	4.092MHz	1bit CMOS	1	1	1

Note: for the Reference frequency selection, the '0' state represents a connection to GND. These are pre-configured default states. Other output formats such as formatted serial or other frequency plans are available through 3 –wire SPI control. Please contact Rakon for these specialised options.

5.3 Power control

An IDLE_ input allows selection of a low power mode, in which only the TCXO is operating. In this mode the TCXO output is available on the CLK-OUT pin (Pin 10). If the SHDN_ pin is held low the internal circuit is turned off and only the TCXO is running. The TCXO output is always available at Pin 5 OSC_OUT.



5.4 Analogue to Digital Converter and AGC

In the 2bit default modes the IF signal is digitised by a 2-bit sign/magnitude AD converter. The SGN and MAG represent the sign and the magnitude of the digitised IF signal. The four possible levels are coded as shown in Table 7.0.

7.0 SGN	Coded output signal	
	MAG	Value
0	1	+3
0	0	+1
1	0	-1
1	1	-3

The AGC uses the MAG signal as the regulation variable, and sets the gain of the IF amplifier to achieve a “high” state on the MAG output for about 33% of the time.

The SGN output may be used as the data output in systems using a 1 bit output and a default mode is provided for this format.

6.0 PCB layout recommendations

The GRM6510 is a sensitive receiver. Although the module is robust and easy to use, normal precautions to minimise interference are necessary. The RF input should be short as possible and made by 50 ohm microstrip with no vias in the path.

Standard PCB materials such as FR4 can be used. It is recommended to leave some spacing (at least 0.3mm) between the digital output tracks and the ground track to minimise capacitance. These output tracks should be as short as possible and routed away from the module and away from the RF input.

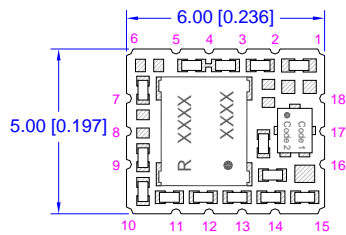


7.0 PIN OUT DESCRIPTION

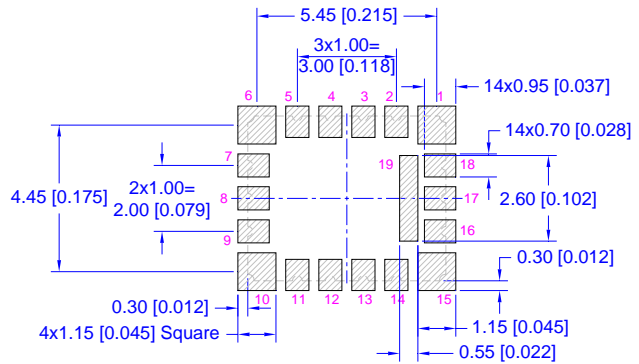
Pin No	Name	Description	Comment
1	DNC	Do Not Connect	Do not make a connection to this pin.
2	$\overline{\text{PGM_CNTL}}$	Program Control	Logic High for default program states or Ground for serial output mode.
3	LNA_IN2	Input for LNA2	RF input for antenna signal. Can connect directly to active antenna, providing bias feed.
4	$\overline{\text{IDLE}}$	Power control logic input	Logic High to enable all functions; logic Low enables oscillator and CLK_OUT only.
5	OSC_OUT	Oscillator Output	A DC connection to the TCXO output
6	I1_OUT/SGN	I1 Data Output	SIGN output to Base band or serial data output to processor (serial mode).
7	IO_OUT/MAG	IO Data Output	MAG output to Base band or data clock output to processor (serial mode).
8	Q0_OUT	Q0 Data Output	
9	Q1_OUT	Q1 Data Output	
10	CLK_OUT	GPS Clock Output	GPS Clock output normally used with SGN/MAG to base band. It can be programmed to be a multiple or sub-multiple of the TCXO frequency if desired.
11	GND_1	Ground 1	Connect to Ground
12	+VCC	Supply Voltage	Connect to a well filtered and regulated supply voltage
13	$\overline{\text{CS}}$	Chip Select	Logic input of 3-wire serial interface. Set low to allow serial data in. Set High when loading has been completed.
14	CLK	Clock for 3-wire serial I/F	Active when CS is low. Data is clocked in on the rising edge of the CLK
15	DATA	Data input for 3-wire serial I/F	
16	$\overline{\text{SHDN}}$	Shut down	A logic low shuts off all but the TCXO.
17	GND_2	Ground 2	Connect to ground
18	ANT_FLAG	Antenna flag	A logic high indicates that an active antenna is connected to the LNA2_IN pin
19	GND_3	Ground 3	Connect to ground



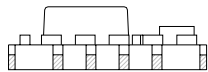
8.0 MODEL DRAWING



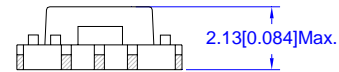
TOP VIEW



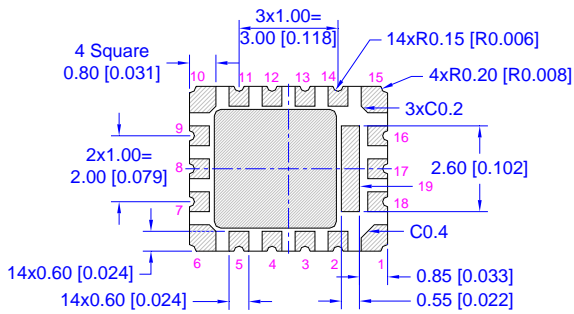
TOP VIEW
RECOMMENDED PAD LAYOUT



SIDE VIEW



END VIEW



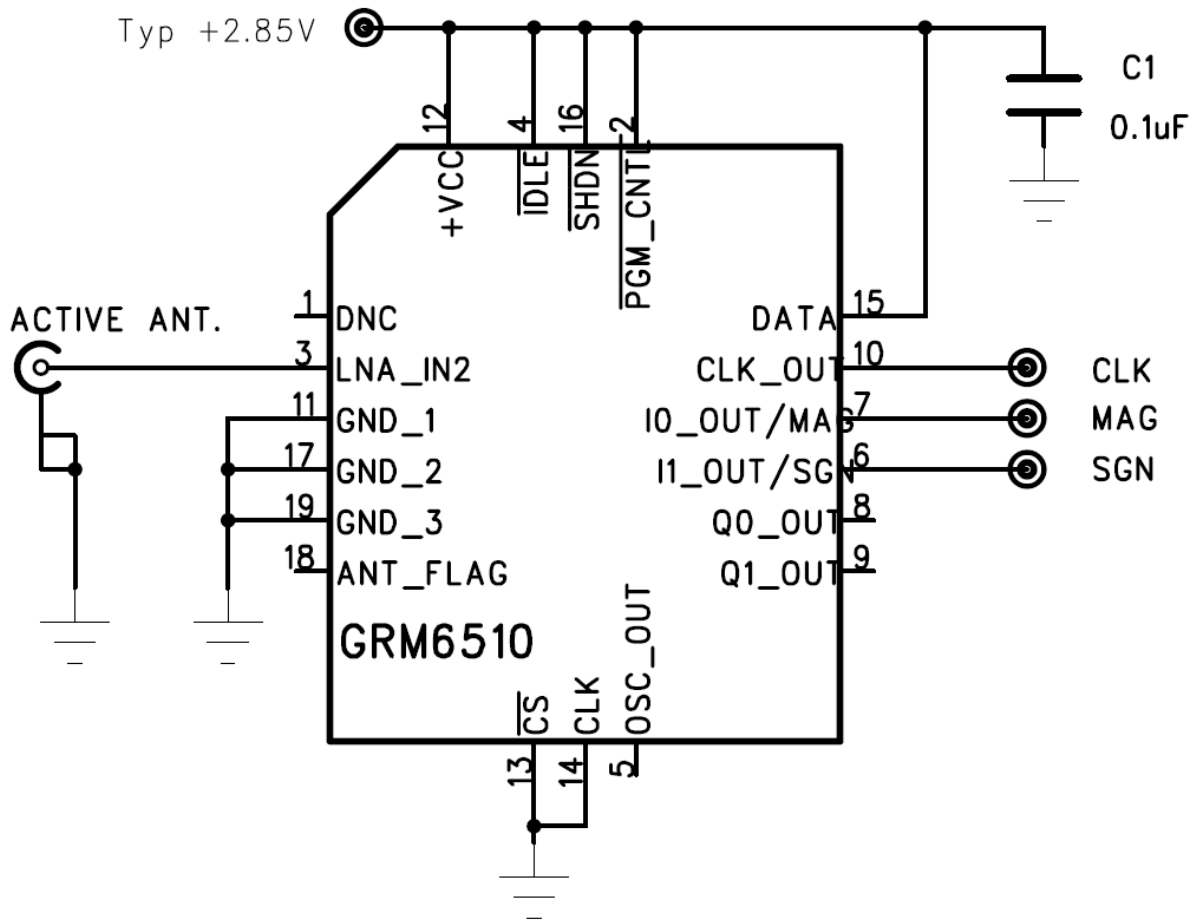
BOTTOM VIEW

PIN CONNECTIONS

1 DNC	11 GND_1
2 PGM_CNTL	12 +VCC
3 LNA_IN2	13 CS
4 IDLE	14 CLK
5 OSC_OUT	15 DATA
6 I1_OUT/SGN	16 SHDN
7 I0_OUT/MAG	17 GND_2
8 Q0_OUT	18 ANT_FLAG
9 Q1_OUT	19 GND_3
10 CLK_OUT	



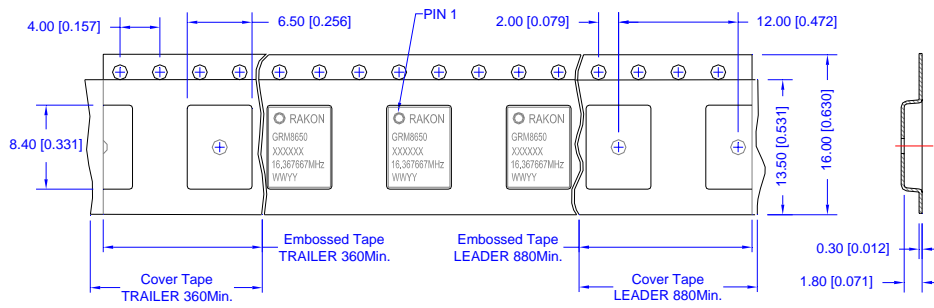
9.0 APPLICATION CIRCUIT DRAWING



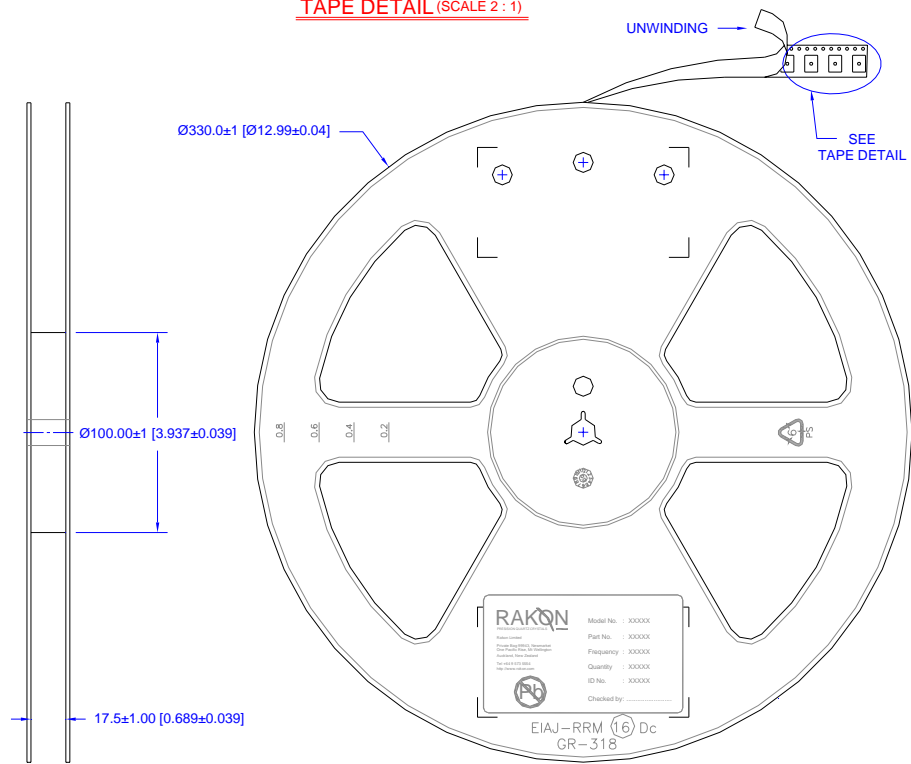
This is an application circuit for connection to a base band and an active antenna. Default mode shown for reference frequencies typically in the range 16.367MHz to 16.368MHz.



10.0 TAPE & REEL DRAWING



TAPE DETAIL (SCALE 2 : 1)

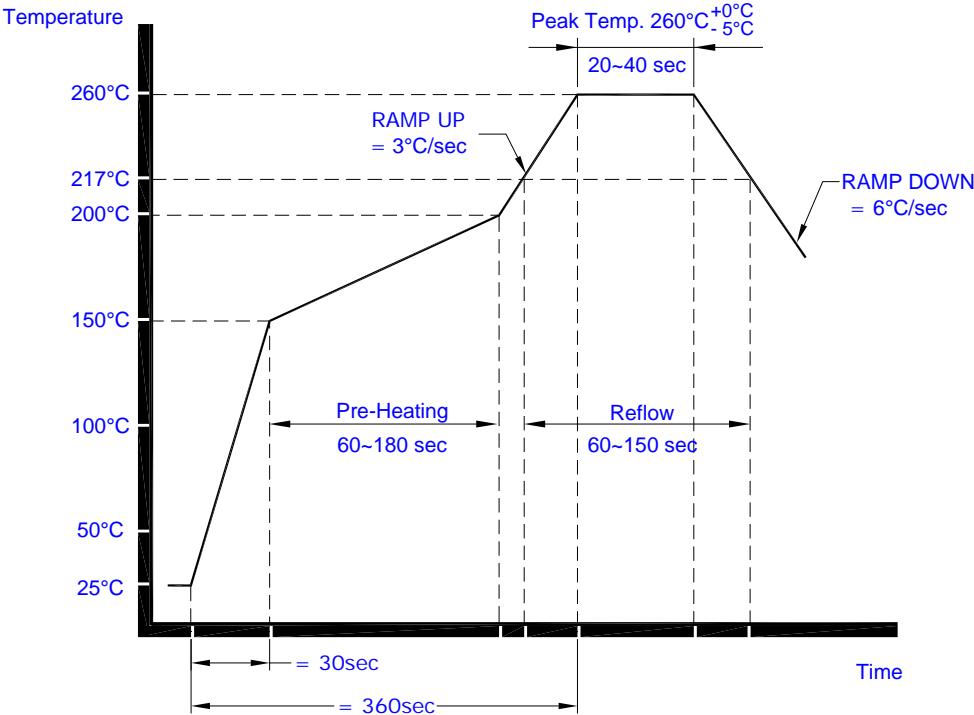


REEL DETAIL (SCALE 1 : 5)

NOTE: Ø330mm REEL'S STANDARD PACKING QUANTITY IS 2000 UNITS PER REEL.



11.0 REFLOW DRAWING



NOTE: The product has been tested to withstand the Reflow Profile shown. The Reflow Profile used to solder the device is determined by the solder paste Manufacturer's specification. It is recommended that the Reflow Profile used does not exceed the one shown in this picture.