

GRM8650 PRELIMINARY

High Sensitivity RF Front-End Module for GNSS systems using Hardware* base bands

The Rakon GRM8650 is a complete miniature RF Front-End including a high dynamic range LNA and SAW filter giving excellent performance on passive antennas. The module translates L1-band signals to a filtered 4 MHz IF frequency which is converted to a 2bit data format for connection to the base band.

Product Description

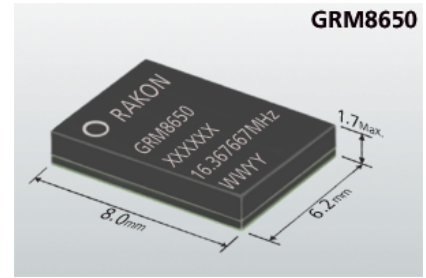
The GRM8650 provides a 'glue-less' solution for the front-end function in a GNSS product using a hardware base band. A precision 0.5ppm TCXO is fitted to ensure rapid acquisition over a wide temperature range.

The module has a 1.8dB typical cascaded noise figure and high dynamic range, suitable for demanding RF environments or co-location with transceivers. The built-in LNA and SAW filter enables the module to be used directly with a passive antenna. Using an image rejecting mixer, the converter supports Galileo signals simultaneously with GPS ready for dual-mode products.

A default setting* for the low power synthesiser is normally used to allow a reference frequency in the common 16.368MHz or 19.2MHz ranges to be fitted, and the frequency required must be specified when ordering. An on-chip AGC frees the base-band system from the overhead of gain adjustment.

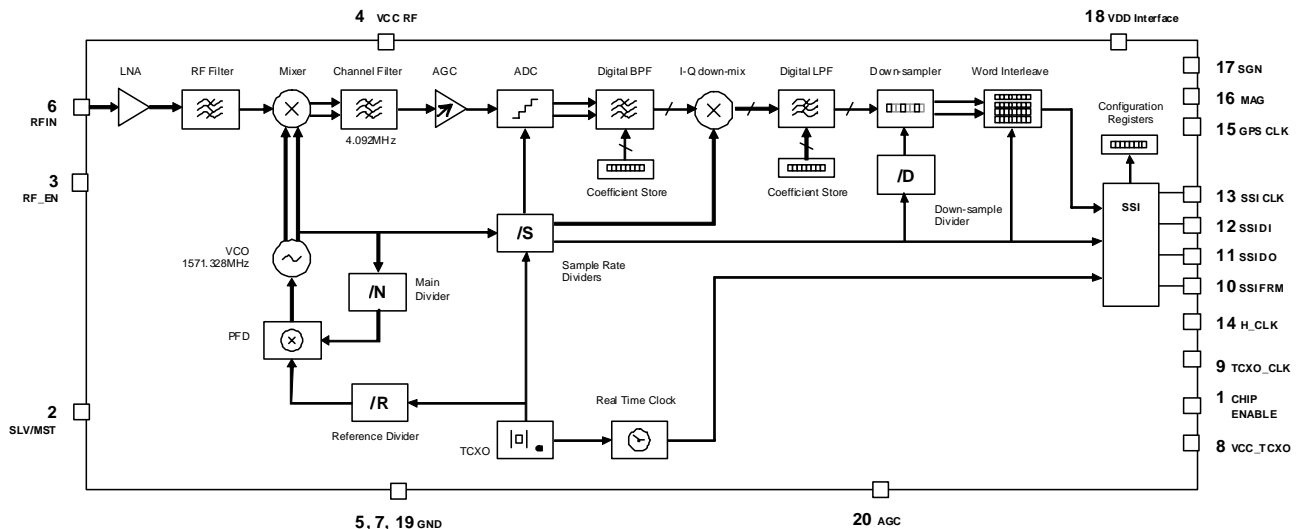
A separate high-impedance chip select input reduces quiescent current leakage below 10µA. The module can be powered from supplies between 2.56V and 3.0V with the interface independently operating between 1.7V and 3.0V.

* This module can be programmed for different settings on the SSI control lines in SPI fashion if desired. It can also be programmed for a streaming output to a host processor for software derived base band applications. Detail on this is given in another version of this specification intended for software GNSS. This is normally provided under NDA.



Features

- Complete tested L1 frequency GNSS receiver*
- Reduces time to market as no receiver design time needed*
- Simplifies product BOM and purchasing requirements*
- 1.8dB cascaded NF allows use with passive antennas*
- Interfaces easily between antenna and base band by direct connection*
- Built in LNA and SAW filter*
- Suitable for both GPS and Galileo*
- 2-bit resolution*
- Choice of TCXO timing references with stabilities down to 0.5ppm*
- 2.56V – 3.0V supply*
- 1.7V – 3.0V interface*
- Supply current: 27mA fully active, 2mA TCXO only*
- 8mm x 6mm x 1.8mm package*





Pin Description

RFIN (6)

The RF input pad is AC coupled internally to an LNA which is designed to give the lowest noise performance for a 50 ohm nominal source impedance. The performance is excellent with a direct connection to a passive antenna or a phantom powered active external antenna can be used if desired. Additional ESD protection may be desired where the end user has access to the RF input.

CHIP_EN (1) Active HI input

When CHIP_EN is set LO, all sections are disabled and so CHIP_EN must remain HI (VDD Interface voltage) during active operation.

When the CHIP_EN input is set HI, the RF sections can be activated under control of the RF_EN (see below).

A LO to HI transition on CHIP_EN resets all registers to their default values.

RF_EN (3) Active HI input

When RF_EN is set HI (VDD Interface voltage), the RF section of the module including the LNA is enabled. This input allows these RF sections to be shut down to leave just the TCXO running if desired to save power.

VCC_TCXO (8)

The power supply for the TCXO is drawn from the independent VCC_TCXO pin. In most applications this pin would be driven in common with the CHIP_EN pin and must be HI whenever CHIP_EN is HI. When both CHIP_EN and VCC_TCXO are set LO, the module current consumption is reduced to below 10µA.

When HI, the VCC_TCXO pin must be supplied with a minimum of 2.5V and draws no more than 2mA.

H_CLK (14) Output

Not used in default mode and should not be connected.

TCXO_CLK (9) Output

A master clock from the module TCXO frequency reference is available for peripheral devices. TCXO_CLK is available whenever VCC_TCXO is HI. TCXO_CLK is a pseudo-sine wave output and is DC coupled to this pin.

SLV/MST (2) Input

Must be tied HI to the VDD Interface voltage (pin 18)

SGN (17) Output

SGN delivers the SIGN output of the ADC whenever RF_EN is HI. Connect to the base band input.

MAG (16) Output

MAG delivers the MAG output of the ADC whenever RF_EN is HI. Connect to the base band input.

GPS_CLK (15) Output

Data from SGN and MAG are valid on positive going edges of GPS_CLK. The rate of GPS_CLK is equal to the ADC sample rate. Connect to the base band clock input.

SSI_CK (13) Input

Connect to Ground.

SSI_FRM (10) Input

Connect to VDD Interface voltage*

SSI_DO (11) Output

Do not connect*

SSI_DI (12) Input

Connect to Ground*

* Note that the synthesiser is flexible, and so can be programmed away from the default mode by additional signalling on the SSI control lines in SPI fashion if desired. Detail on this is given in a version of this specification intended for software GNSS applications (normally supplied under NDA).

PIN OUT DESCRIPTION for GRM8650 in default mode

Pin No	Name	Description	Comment
1	CHIP_EN	Resets and enables the module	Raise to VDD Interface (pin 18) to start module
2	SLV/MST	Interface mode at reset, Slave or Master	Connect to VDD Interface (pin 18) to define as Slave
3	RF_EN	RF enable	Raise to VDD Interface (pin 18) to fully enable receiver
4	VCC RF	Power supply	
5	GND	Ground	RF ground
6	RFIN	Antenna input	AC-coupled inside module
7	GND	Ground	RF ground
8	VCC_TCXO	Oscillator supply	Supplies and enables reference oscillator and TCXO_CLK output
9	TCXO_CLK	Oscillator output	Clipped sine reference oscillator output available whenever VCC_TCXO is HI. AC-couple externally.
10	SSI_FRM	Interface frame signal	Connect to VDD Interface (pin 18)
11	SSI_DO	Interface data signal from module	Do not connect
12	SSI_DI	Interface data signal to module	Connect to Ground
13	SSI_CLK	Interface clock signal	Connect to Ground
14	H_CLK	Interface clock signal from module	Do not connect
15	GPS_CLK	Sample clock	Use in conjunction with SGN and MAG
16	MAG	Sample output (2-bit interface)	Connect to base band
17	SGN	Sample output sign bit	Connect to base band
18	VDD Interface	Supply for digital interfaces and I/O	Connect to the appropriate base band supply to ensure the correct interface voltages. This is the interface voltage for CHIP_EN, SLV/MST, RF_EN, and the synchronous serial interface.
19	GND	Ground	
20	AGC	AGC monitor/External AGC	Please leave un-connected (refer to Sales for special applications)



Absolute Maximum Ratings					
Parameter	Comments	Minimum	Maximum	Units	
VCC VDD Supply Voltage	All supply voltages	-0.3	3.3	V	
TSTG Temperature	Storage Temperature	-60	+150	°C	

Thermal Characteristics					
Parameter	Comments	Minimum	Typical	Maximum	Units
TAMB Temperature	Ambient operating temperature	-40		+85	°C

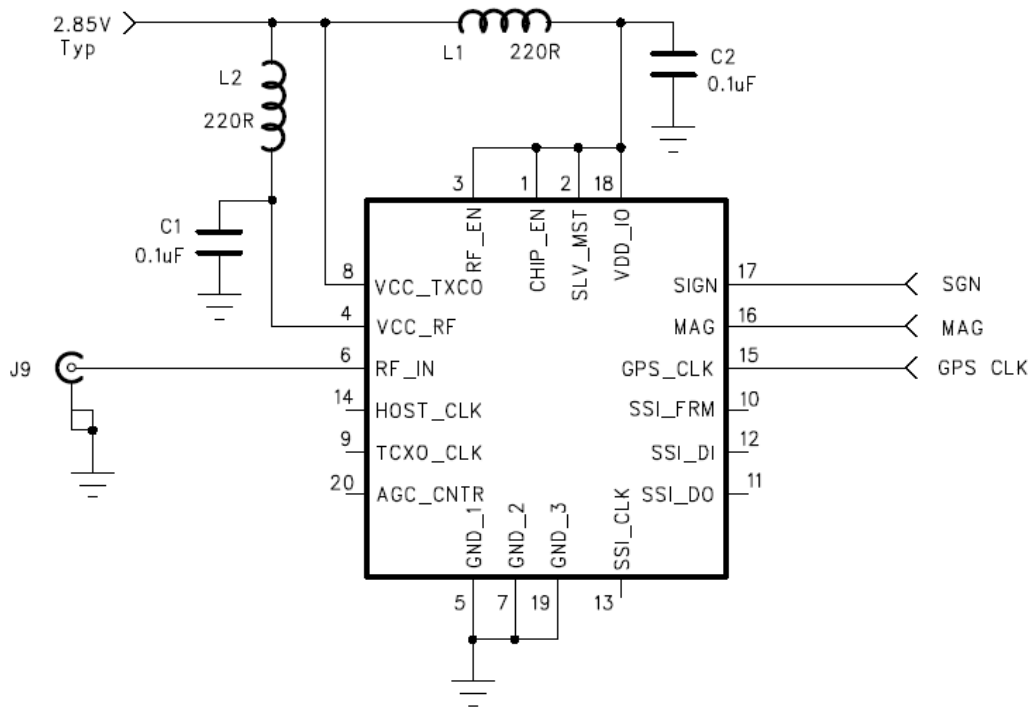
DC Characteristics					
Parameter	Comments	Minimum	Typical	Maximum	Units
VCC Supply Voltage	RF sub-system	2.56		3.0	V
VDD Supply Voltage	Interface	1.7		3.0	V
IVCC Supply Current	Fully Active CHIP_EN =1 (VDD IO), RF_EN =1 (VDDIO)	(2.7V)	27	29	mA
IVCC Supply Current	Time-keeping mode CHIP_EN =1(VDDIO), RF_EN =0	VCC (2.7V) VCC_TCXO (2.7V)	1.5 1.0		mA
IVCC Supply Current	Quiescent CHIP_EN =0		1		µA
II/O Control Input	Digital input current drain CHIP_EN, RF_EN, LNA_EN, SLV/MST, SSI...	-10		10	nA

AC Characteristics					
at 2.7V, 25°C unless specified otherwise					
Parameter	Comments	Minimum	Typical	Maximum	Units
NF Noise Figure	Overall system noise figure		1.8		dB
ΔG Gain Range	AGC gain control range		50		dB
PSD Power Density	Input power spectral density range <1dB compression			-145	dBm/ Hz
P1dB	1dB compression f < 1540MHz, f > 1620MHz		-10		dBm
IIP3	Input-referred third order intercept f1 and f2 < 1540MHz, f1 and f2 > 1620MHz 2.f1 - f2 = 1575.42MHz		3		dBm
SEL Selectivity	Selectivity fLO±12MHz	20			dB
IR Image Rejection	Image rejection fLO-6MHz - fLO-2MHz			20	dB
PN Phase Noise	Phase Noise	1kHz 100kHz	-70	-80	dBc/ Hz
GDD Group Delay	Pass-band group delay variation fLO+2MHz - fLO+6MHz			±70	nsec
t _r Rise Time	All outputs, 10pF load register bit HSR=1			5	nsec
t _f Fall Time	All outputs, 10pF load register bit HSR=1			5	nsec



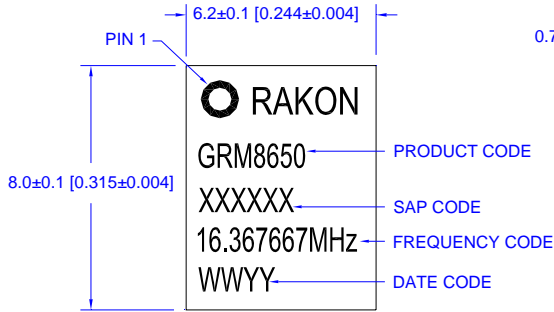
Settling Times					
Parameter	Comments	Minimum	Typical	Maximum	Units
TOSC1 Oscillator Start	Frequency within 1% after CHIP_EN=1 (VDDIO), VCC_TCXO=HI			1	msec
TOSC2 Oscillator Start	Frequency within specification after CHIP_EN= 1 (VDD IO), VCC_TCXO=HI			100	msec
TREC Receiver Start	Receiver settling time after RF_EN=HI (VDDIO)			1	msec
TAGC AGC Settling	AGC recovery time from saturation			100	µsec

Application circuit

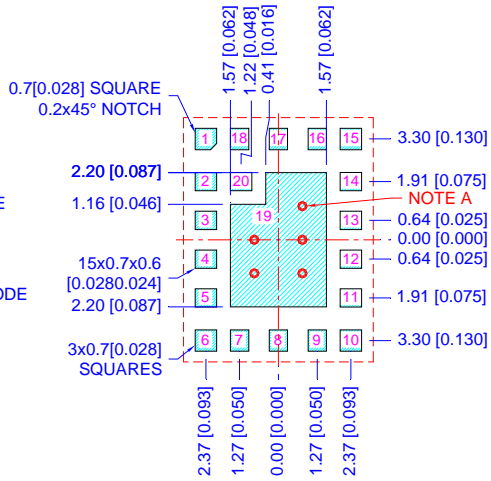


Reference Circuit for Hardware GNSS

Model Drawing

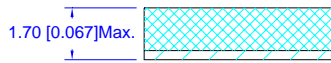


TOP VIEW

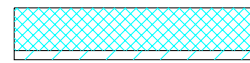


RECOMMENDED PAD LAYOUT

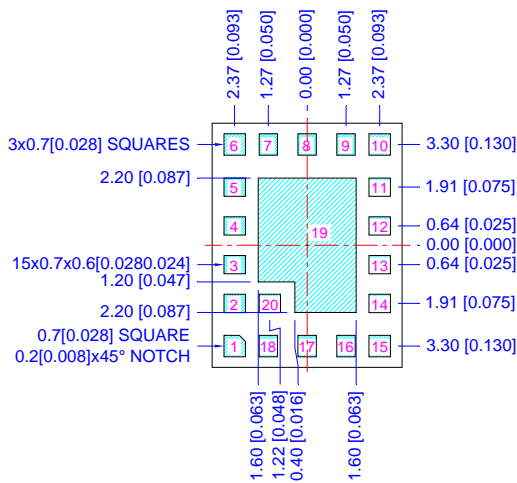
NOTE A: LAYER BELOW SHOULD BE GROUND PLANE.
5 VIAS MINIMUM TO THAT PLAN



SIDE VIEW



END VIEW

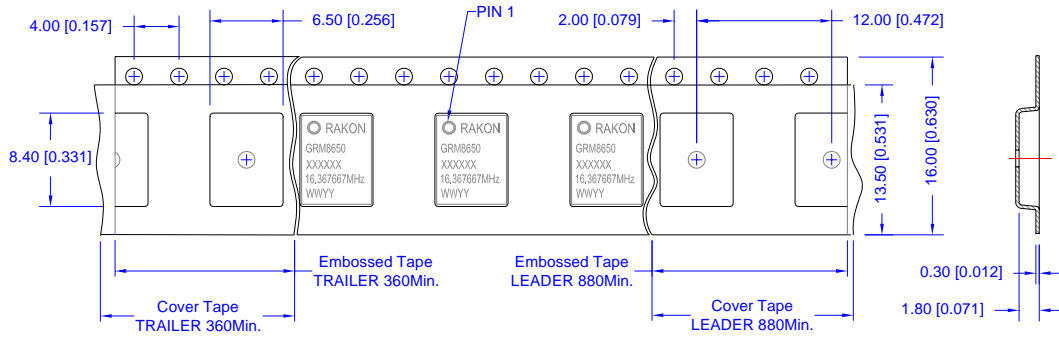


BOTTOM VIEW

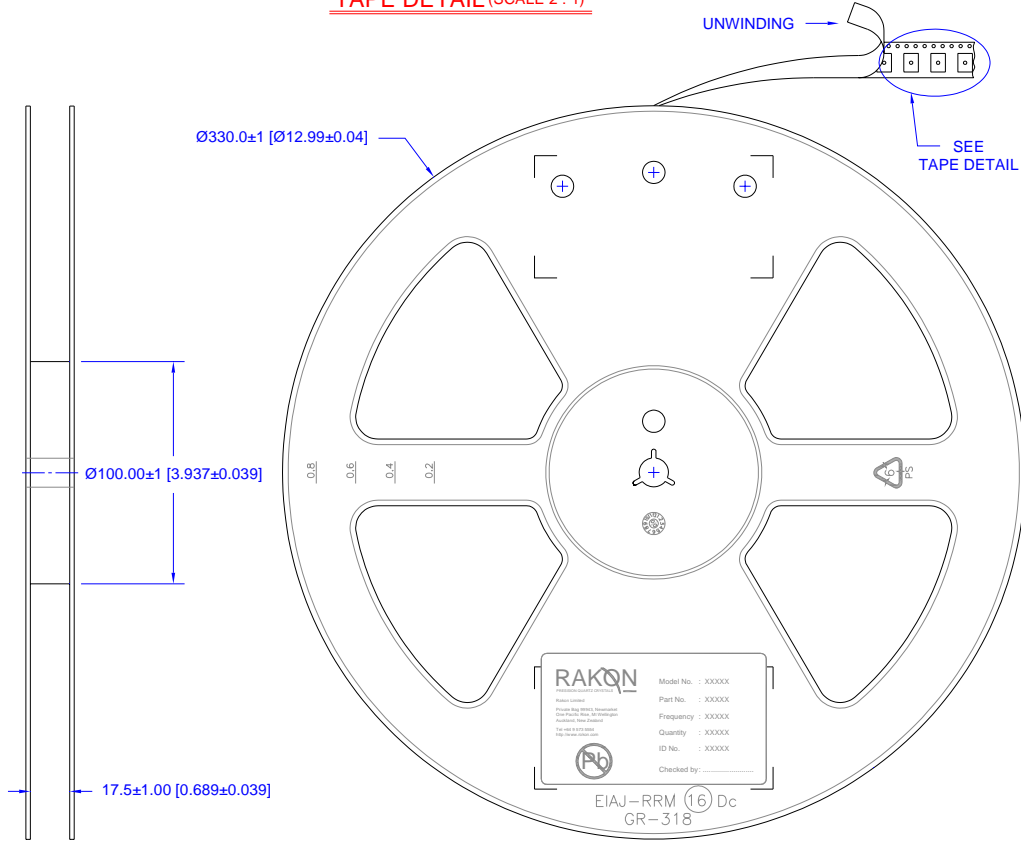
PIN CONNECTIONS			
1	CHIP_EN	11	SSL_DO
2	SLV/MST	12	SSL_DI
3	RF_EN	13	SSL_CLK
4	VCC RF	14	H_CLK
5	GND	15	GPS_CLK
6	RFIN	16	MAG
7	GND	17	SGN
8	VCC_TCXO	18	VDD Interface
9	TCXO_CLK	19	GND
10	SSL_FRM	20	AGC



Tape and Reel Information



TAPE DETAIL (SCALE 2 : 1)

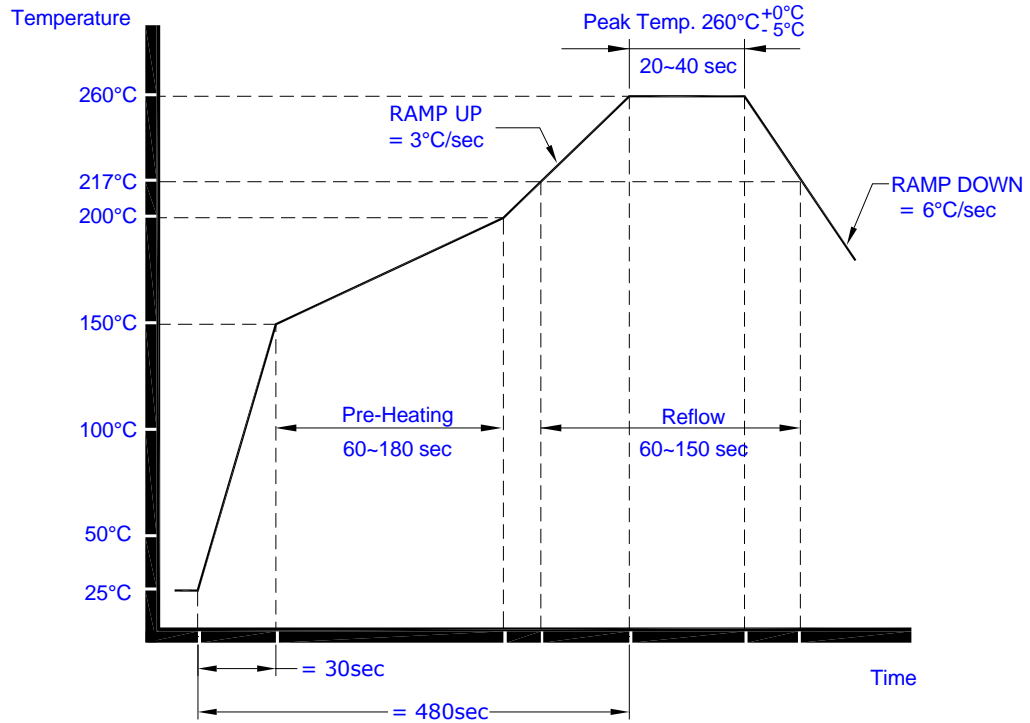


REEL DETAIL (SCALE 1 : 5)

NOTE: ø330mm REEL'S STANDARD PACKING QUANTITY IS 2000 UNITS PER REEL.



Reflow diagram



NOTE: The product has been tested to withstand the Reflow Profile shown. The Reflow Profile used to solder the device is determined by the solder paste Manufacturer's specification. It is recommended that the Reflow Profile used does not exceed the one shown above.