

RS7500P XO



Overview

'Panther' High performance PLL based XO in 7 x 5 mm Surface Mount package.

Description

This PLL based frequency multiplication XO offers ultra low RMS phase jitter, and high frequency stability in an industry standard 7 x 5 mm SMD package.

Recommended Applications

Consumer Products, DSL/ADSL, Ethernet, SONET/SDH, WiFi, WiMAX/WLAN, Communications, Other.

Form factor

7 x 5 mm

RS7500P XO Specifications

1.0 Specification References

1.1	Model Description	RS7500P XO (Preliminary)
1.2	RoHS Compliant	Yes
1.3	Reference Number	
1.4	Custom P#	
1.5	Output Enable Connection	1) Pad 1, 2) Pad 2, 3) N/C - please state only one option

2.0 Frequency Characteristics

Parameter	Test Condition	Value	Units
2.1	Frequency Range	Frequency range available	10 to 800 MHz
2.2	Operating Temperature Range	(Note 1)	-40 to 85 °C
2.3	Frequency Stability	Including Temp. range, Supply variation, Load variation and 15 years aging	15 to 50 ±ppm

3.0 Power Supply

Parameter	Test Condition	Value	Units
3.1	Supply Voltage	With a tolerance of ±10%	3.3 max V
3.2	Supply Current	(Note 2)	10 to 120 mA

4.0 Output Characteristic - LVPECL Only

Parameter	Test Condition	Value	Units
4.1	Output	LVPECL	
4.2	Duty Cycle	@ VCC-1.3 V	45 to 55 %
4.3	Output Load	With VCC-2 V @ 50 Ω	
4.4	Rise time/Fall time	80%/20% (Note 3)	0.5 to 3 ns
4.5	Tristate High on Pad 1 or 2	Output disabled (>70% of VCC or GND) (Note 4)	
4.6	Tristate Low on Pad 1 or 2	Output enabled (<30% of VCC or open) (Note 4)	
4.7	RMS Phase Jitter	Integrated 12 KHz to 20 MHz. Typical @ 155.52 MHz (Note 5)	0.5 ps
4.8	RMS Period Jitter	Typical @ 155.52 MHz (Note 5)	3 ps
4.9	Sub-Harmonics		-40 max dBc

5.0 Output Characteristic - LVCMOS Only

Parameter	Test Condition	Value	Units
5.1	Output	LVCMOS	
5.2	Duty Cycle	@ 50% VCC	45 to 55 %
5.3	Output Load		15 to 50 pF
5.4	Rise time/Fall time	90%/10% (Note 3)	0.5 to 3 ns
5.5	Tristate High on Pad 1 or 2	Output enabled (>70% of VCC or GND) (Note 4)	
5.6	Tristate Low on Pad 1 or 2	Output disabled (<30% of VCC or open) (Note 4)	
5.7	RMS Phase Jitter	Integrated 12 KHz to 20 MHz. Typical @ 155.52 MHz (Note 5)	0.5 ps
5.8	RMS Period Jitter	Typical @ 155.52 MHz (Note 5)	3 ps
5.9	Sub-Harmonics		-40 max dBc

6.0 Output Characteristic - LVDS Only

Parameter	Test Condition	Value	Units
6.1 Output	LVDS		
6.2 Duty Cycle	Measured at 1.25 V	45 to 55	%
6.3 Output Load	RL = 100 Ω / CL = 10 pF		
6.4 Rise time/Fall time	RL = 100 Ω / CL = 10 pF (Note 3)	0.5 to 3	ns
6.5 Tristate High on Pad 1 or 2	Output enabled (>70% of VCC or GND) (Note 4)		
6.6 Tristate Low on Pad 1 or 2	Output disabled (<30% of VCC or open) (Note 4)		
6.7 RMS Phase Jitter	Integrated 12 KHz to 20 MHz. Typical @ 155.52 MHz (Note 5)	0.5	ps
6.8 RMS Period Jitter	Typical @ 155.52 MHz (Note 5)	3	ps
6.9 Sub-Harmonics		-40 max	dBc

7.0 SSB Phase Noise

Parameter	Test Condition	Value	Units
7.1 SSB Phase Noise power density @ 10 Hz offset	Value for a 24.576 MHz XO @ 25 °C	-75 max	dBc/Hz
7.2 SSB Phase Noise power density @ 100 Hz offset	Value for a 24.576 MHz XO @ 25 °C	-100 max	dBc/Hz
7.3 SSB Phase Noise power density @ 1 KHz offset	Value for a 24.576 MHz XO @ 25 °C	-125 max	dBc/Hz
7.4 SSB Phase Noise power density @ 10 KHz offset	Value for a 24.576 MHz XO @ 25 °C	-140 max	dBc/Hz
7.5 SSB Phase Noise power density @ 100 KHz offset	Value for a 24.576 MHz XO @ 25 °C	-145 max	dBc/Hz

8.0 SSB Phase Noise

Parameter	Test Condition	Value	Units
8.1 SSB Phase Noise power density @ 10 Hz offset	Value for a 155.52 MHz XO @ 25 °C	-62 max	dBc/Hz
8.2 SSB Phase Noise power density @ 100 Hz offset	Value for a 155.52 MHz XO @ 25 °C	-92 max	dBc/Hz
8.3 SSB Phase Noise power density @ 1 KHz offset	Value for a 155.52 MHz XO @ 25 °C	-120 max	dBc/Hz
8.4 SSB Phase Noise power density @ 10 KHz offset	Value for a 155.52 MHz XO @ 25 °C	-132 max	dBc/Hz
8.5 SSB Phase Noise power density @ 100 KHz offset	Value for a 155.52 MHz XO @ 25 °C	-128 max	dBc/Hz

9.0 SSB Phase Noise

Parameter	Test Condition	Value	Units
9.1 SSB Phase Noise power density @ 10 Hz offset	Value for a 622.08 MHz XO @ 25 °C	-49 max	dBc/Hz
9.2 SSB Phase Noise power density @ 100 Hz offset	Value for a 622.08 MHz XO @ 25 °C	-84 max	dBc/Hz
9.3 SSB Phase Noise power density @ 1 KHz offset	Value for a 622.08 MHz XO @ 25 °C	-111 max	dBc/Hz
9.4 SSB Phase Noise power density @ 10 KHz offset	Value for a 622.08 MHz XO @ 25 °C	-120 max	dBc/Hz
9.5 SSB Phase Noise power density @ 100 KHz offset	Value for a 622.08 MHz XO @ 25 °C	-118 max	dBc/Hz

10.0 Environmental

Parameter	Test Condition
10.1 Mechanical Shock	MIL-STD-883, Method 2002
10.2 Storage Temperature Range	-55 to 125 °C
10.3 Humidity	After 48 hours at 85 °C±2 °C 85 % relative humidity non-condensing
10.4 Thermal Shock	MIL-STD-883, Method 1011
10.5 Vibration	MIL-STD-883, Method 2007
10.6 Gross and Fine Leak	MIL-STD-883, Method 1014

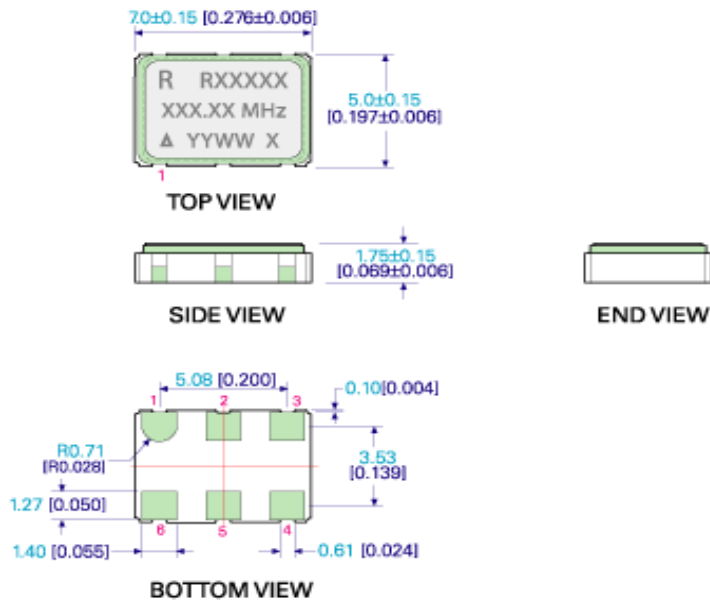
11.0 Manufacturing Information

Parameter	Test Condition
11.1 Packaging description	Refer to packaging information
11.2 Reflow	Solder reflow process as per attached profile

12.0 Specification Notes

Parameter	Test Condition
13.1 Note 1	The operating temperature range needs to be specified
13.2 Note 2	Output current depends on the frequency selected and the output characteristics chosen
13.3 Note 3	The exact value will be frequency dependant
13.4 Note 4	Enable high and low is available as an option. This feature can be configured for either Pad 1 or Pad 2
13.5 Note 5	The jitter values will vary depending on the frequency selected

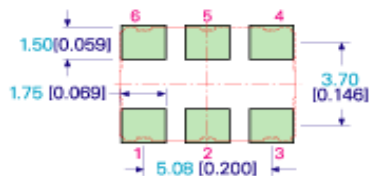
MODEL DRAWING



PIN CONNECTIONS

PIN	XO		VCXO	
	LVC MOS	LVPECL/LVDS	LVC MOS	LVPECL/LVDS
1	E/D or NC	E/D or NC	VCO	VCO
2	E/D or NC	E/D or NC	E/D	E/D
3	GND	GND	GND	GND
4	OUTPUT	OUTPUT	OUTPUT	OUTPUT
5	N/C	OUTPUT	N/C	OUTPUT
6	VCC	VCC	VCC	VCC

RECOMMENDED PAD LAYOUT - TOP VIEW



TITLE: PLL 7500P MODEL

RELATED DRAWINGS:

PRELIMINARY

FILENAME: CAT175

REVISION: A

DATE: 25-Mar-09

SCALE: 5 : 1

Millimetres [inch]

Tolerance:

XX = ±0.5

X.X = ±0.2

X.XX = ±0.10

X.XXX = ±0.05

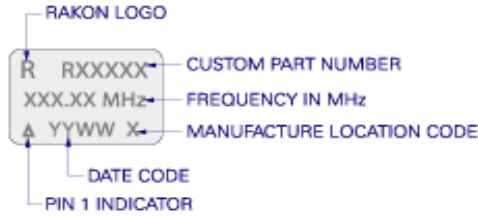
X^o = ±1.0°

Hole = ±0.10

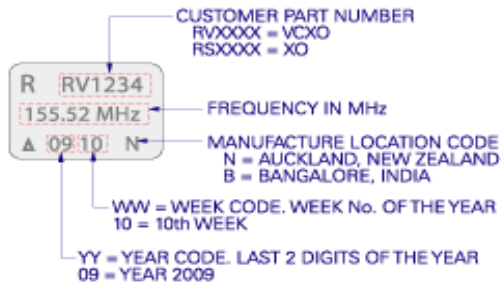
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VCXO / XO7500 LID MARKING



LASER MARKING EXAMPLE



TITLE: VCXO7500 SERIES LID MARKING

RELATED DRAWINGS:

PRELIMINARY

FILENAME: CAT069

REVISION: A1

DATE: 07-Apr-09

SCALE: NTS

Millimetres [inch]

Tolerances:

XX = ±0.5

X.X = ±0.2

X.XX = ±0.10

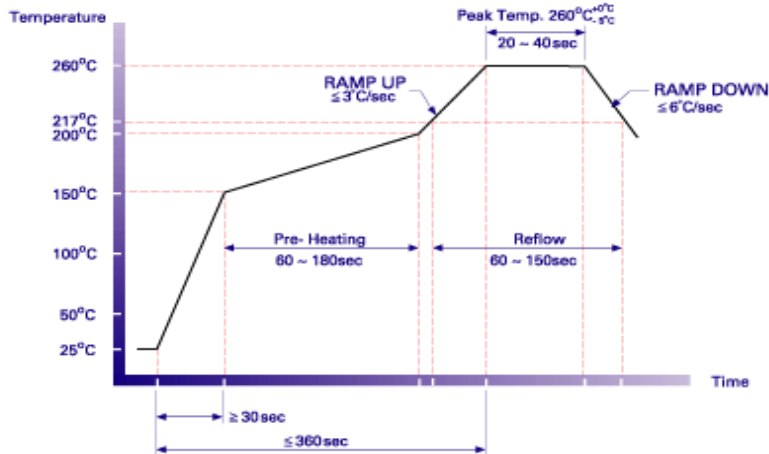
X.XXX = ±0.05

X° = ±1.0°

Hole = ±0.10

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NOTE:

The product has been tested to withstand the Reflow Profile shown. The Reflow Profile used to solder Rakon VCXO/XO is determined by the solder paste manufacturer's specification. It is recommended that the Reflow Profile used does not exceed the one shown above.

TITLE: VCXO7500 SERIES Pb-FREE REFLOW

RELATED DRAWINGS:

FILENAME: CAT033

REVISION: A

DATE: 30-Mar-09

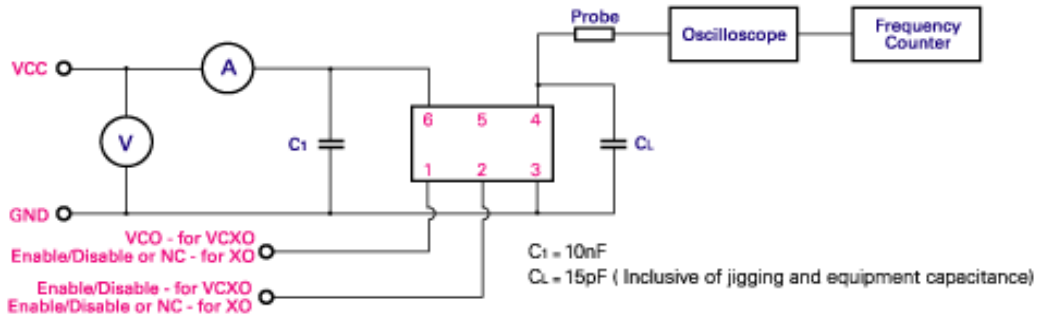
SCALE: NTS

Millimetres [inch]

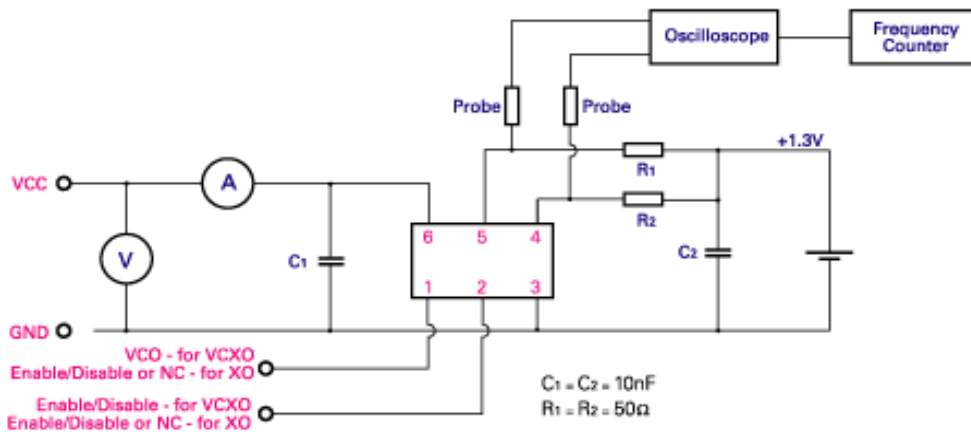
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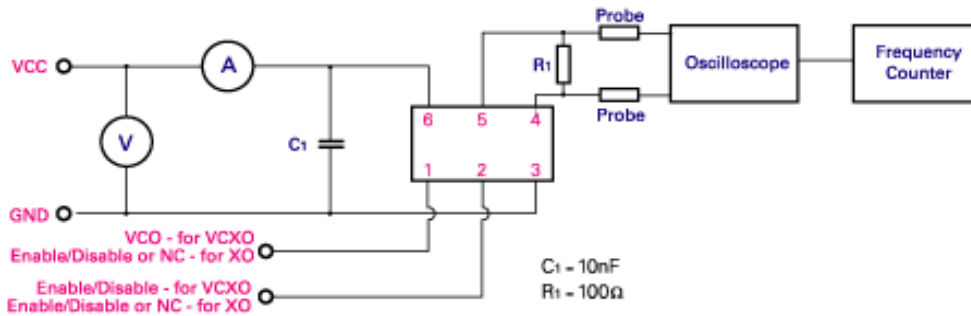
LVCMOS TEST CIRCUIT :



LVPECL TEST CIRCUIT :



LVDS TEST CIRCUIT :



TITLE: VCXO7500 SERIES TEST CIRCUIT

RELATED DRAWINGS:

FILENAME: CAT088

REVISION: A

DATE: 03-Apr-09

SCALE: NTS

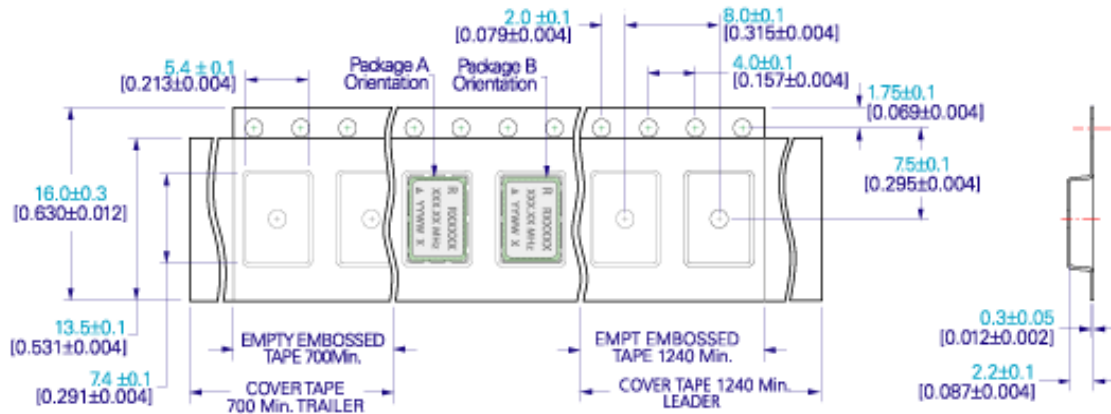
Millimetres [inch]

PRELIMINARY

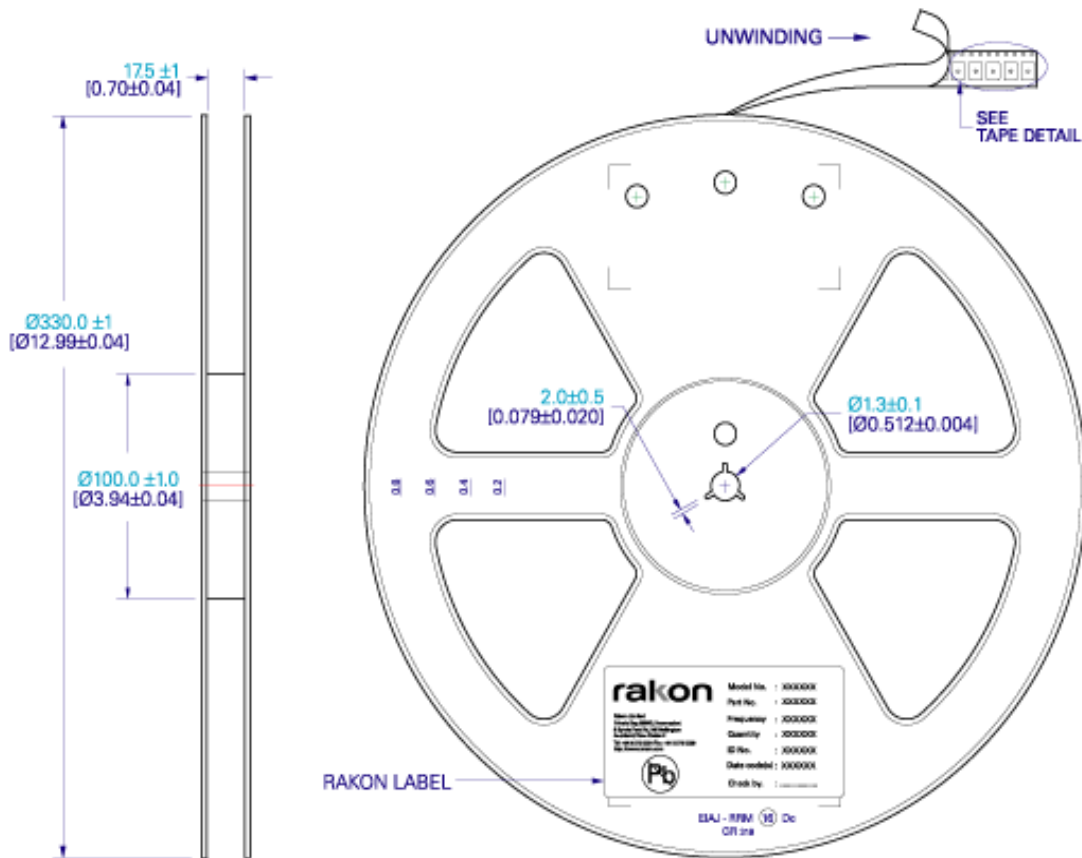
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TAPE DETAIL (SCALE 2 : 1)



REEL DETAIL (SCALE 1 : 5)



NOTE: Ø330mm REEL'S STANDARD PACKING QUANTITY IS 2000 OSCILLATORS PER REEL.

TITLE: VCXO7500 Pb-free TAPE & REEL

RELATED DRAWINGS:

FILENAME: CAT032

REVISION: A

DATE: 30-Mar-09

SCALE: See above

Millimetres [inch]

Tolerance:

XX = ±0.5

X.X = ±0.2

X.XX = ±0.10

X.XXX = ±0.05

X^o = ±1.0°

Hole = ±0.10

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