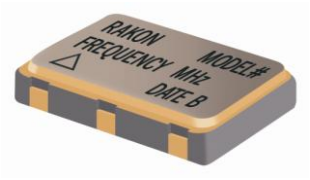
RV7500P



Overview

`Panther' High performance PLL based VCXO in 7 x 5 mm Surface Mount Package

Description

This PLL VCXO offers ultra low RMS phase jitter, high linearity pull range and high frequency stability in an industry standard 7 x 5 mm SMD package.

Recommended Applications

Base-station, Ethernet, SONET/SDH, Communications, Other.

Form factor

7 x 5 mm

RV7500P Specifications

1.0 Specification References

1.1	Model Series	RV7500P VCXO 7 x 5 mm (Preliminary)
1.2	RoHS Compliant	Yes
1.3	Reference #	
1.4	Custom #	

2.0 Frequency Characteristics

	Parameter	Test Condition	Value	Units
2.1	Frequency Range		10 to 800	MHz
2.2	Operating Temperature Range	(Note 1)	-40 to 85	°C
2.3	Frequency Stability	Including Temperature range, Supply variation, Load variation & 15 years Aging	15 to 50	±ppm

3.0 Power Supply

	Parameter	Test Condition	Value	Units
3.1	Supply Voltage	With a tolerance of ±10%	3.3 max	V
3.2	Supply Current	(Note 2)	10 to 120	mA

4.0 Control Voltage (VCO)

	Parameter	Test Condition	Value	Units
4.1	Absolute Pulling Range		50 min.	±ppm
4.2	Pulling Range	Frequency shift from minimum to maximum control voltage (Note 3)	40 to 250	±ppm
4.3	Control Voltage	Nominal 1.65V	0 to 3.3	V
4.4	Linearity		10 max	%
4.5	Slope	Positive only	10 to 100	ppm/V
4.6	Modulation BW		0.3 to 100	KHz
4.7	Input Impedance		10 to 2000	MΩ

5.0 Output Characteristics (LVPECL Only)

	Parameter	Test Condition	Value	Units
5.1	Output	LVPECL		
5.2	Duty Cycle	@ VCC-1.3 V	45 to 55	%
5.3	Output Load	With VCC-2 V @ 50 Ω		
5.4	Rise time / Fall time	80%/20% (Note 4)	0.5 to 3	ns
5.5	Tristate High on Pad 2	Output disabled (>70% of VCC or GND) (Note 5)		
5.6	Tristate Low on Pad 2	Output enabled (<30% of VCC or open) (Note 5)		
5.7	RMS Phase Jitter	Integrated 12 KHz to 20 MHz. Typical @ 155.52MHz (Note 6)	0.5	ps
5.8	RMS Period Jitter	Typical @ 155.52 MHz (Note 6)	3	ps
5.9	Sub-Harmonics		-40 max	dBc

6.0 Output Characteristics (LVCMOS Only)

	Parameter	Test Condition	Value	Units
6.1	Output	LVCMOS		
6.2	Duty Cycle	@ 50% VCC	45 to 55	%
6.3	Output Load		15 to 50	pF
6.4	Rise time / Fall time	90%/10% (Note 4)	0.5 to 3	ns
6.5	Tristate High on Pad 2	Output enabled (>70% of VCC or GND) (Note 5)		
6.6	Tristate Low on Pad 2	Output disabled (<30% of VCC or open) (Note 5)		
6.7	RMS Phase Jitter	Integrated 12 KHz to 20 MHz. Typical @ 155.52MHz (Note 6)	0.5	ps
6.8	RMS Period Jitter	Typical @ 155.52 MHz (Note 6)	3	ps
6.9	Sub-Harmonics		-40 max	dBc

7.0 Output Characteristics (LVDS Only)

	Parameter	Test Condition		
7.1	LVDS			
7.2	Duty Cycle	Measured at 1.25 V	45 to 55	%
7.3	Output Load	RL = 100 Ω / CL = 10 pF		
7.4	Rise time / Fall time	RL = 100 Ω / CL = 10 pF (Note 4)	0.5 to 3	ns
7.5	Tristate High on Pad 2	Output enabled (>70% of VCC or GND) (Note 5)		
7.6	Tristate Low on Pad 2	Output disabled (<30% of VCC or open) (Note 5)		
7.7	RMS Phase Jitter	Integrated 12 KHz to 20 MHz. Typical @ 155.52MHz (Note 6)	0.5	ps
7.8	RMS Period Jitter	Typical @ 155.52 MHz (Note 6)	3	ps
7.9	Sub-Harmonics		-40 max	dBc

8.0 SSB Phase Noise

	Parameter	Test Condition		
8.1	SSB Phase Noise power density @ 10 Hz offset	Value for a 24.576 MHz VCXO @ 25 °C	-65	dBc/Hz
8.2	SSB Phase Noise power density @ 100 Hz offset	Value for a 24.576 MHz VCXO @ 25 °C	-100	dBc/Hz
8.3	SSB Phase Noise power density @ 1 KHz offset	Value for a 24.576 MHz VCXO @ 25 °C	-123	dBc/Hz
8.4	SSB Phase Noise power density @ 10 KHz offset	Value for a 24.576 MHz VCXO @ 25 °C	-130	dBc/Hz
8.5	SSB Phase Noise power density @ 100 KHz offset	Value for a 24.576 MHz VCXO @ 25 °C	-125	dBc/Hz

9.0 SSB Phase Noise

	Parameter	Test Condition		
9.1	SSB Phase Noise power density @ 10 Hz offset	Value for a 155.52 MHz VCXO @ 25°C	-62	dBc/Hz
9.2	SSB Phase Noise power density @ 100 Hz offset	Value for a 155.52 MHz VCXO @ 25°C	-92	dBc/Hz
9.3	SSB Phase Noise power density @ 1 KHz offset	Value for a 155.52 MHz VCXO @ 25°C	-120	dBc/Hz
9.4	SSB Phase Noise power density @ 10 KHz offset	Value for a 155.52 MHz VCXO @ 25°C	-132	dBc/Hz
9.5	SSB Phase Noise power density @ 100 KHz offset	Value for a 155.52 MHz VCXO @ 25°C	-128	dBc/Hz

10.0 SSB Phase Noise

	Parameter	Test Condition		
10.1	SSB Phase Noise power density @ 10 Hz offset	Value for a 622.08 MHz VCXO @ 25°C	-48	dBc/Hz
10.2	SSB Phase Noise power density @ 100 Hz offset	Value for a 622.08 MHz VCXO @ 25°C	-80	dBc/Hz
10.3	SSB Phase Noise power density @ 1 KHz offset	Value for a 622.08 MHz VCXO @ 25°C	-108	dBc/Hz
10.4	SSB Phase Noise power density @ 10 KHz offset	Value for a 622.08 MHz VCXO @ 25°C	-118	dBc/Hz
10.5	SSB Phase Noise power density @ 100 KHz offset	Value for a 622.08 MHz VCXO @ 25°C	-114	dBc/Hz

11.0 Environmental

	Parameter	Test Condition
11.1	Mechanical Shock	MIL-STD-883, Method 2002
11.2	Storage Temperature range	-55 to 125 °C
11.3	Humidity	After 48 hours at 85 °C ± 2 °C 85% relative humidity non-condensing
11.4	Thermal Shock	MIL-STD-883, Method 1011
11.5	Vibration	MIL-STD-883, Method 2007
11.6	Gross and Fine Leak	MIL-STD-883, Method 1014

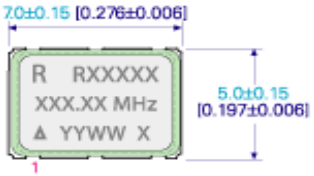
12.0 Manufacturing Information

	Parameter	Test Condition
12.1	Packaging Description	Tape and reel as shown
12.2	Reflow	Solder reflow process as per attached profile

13.0 Specification Notes

	Parameter	Test Condition
13.1	Note 1.	The operating temperature range needs to be specified
13.2	Note 2.	Output current depends on the frequency selected and the output characteristics chosen
13.3	Note 3.	Select the exact tuning range required. The values listed are maximum normally available and may require some trade-off in frequency stability. Standard options are ±50 ppm, ±75 pm, ±100 ppm and ±150 ppm
13.4	Note 4.	The exact value will be frequency dependant
13.5	Note 5.	Enable high or low is available as an option
13.6	Note 6.	The jitter values will vary depending on the frequency selected

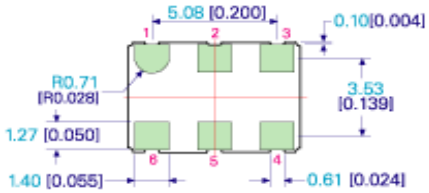
MODEL DRAWING



TOP VIEW

SIDE VIEW

END VIEW

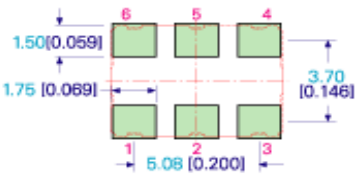


BOTTOM VIEW

PIN CONNECTIONS

PIN	XO		VCXO	
	LVCMOS	LVPECL/LVDS	LVCMOS	LVPECL/LVDS
1	E/D or NC	E/D or NC	VCO	VCO
2	E/D or NC	E/D or NC	E/D	E/D
3	GND	GND	GND	GND
4	OUTPUT	OUTPUT	OUTPUT	OUTPUT
5	N/C	$\overline{\text{OUTPUT}}$	N/C	$\overline{\text{OUTPUT}}$
6	VCC	VCC	VCC	VCC

RECOMMENDED PAD LAYOUT - TOP VIEW



TITLE: PLL 7500P MODEL
RELATED DRAWINGS:

PRELIMINARY

FILENAME: CAT175
REVISION: A
DATE: 25-Mar-09
SCALE: 5 : 1
Millimetres [inch]

Tolerance:
XX ±0.5
X.X ±0.2
X.XX ±0.10
X.XXX ±0.05
X° ±1.0°
Hole ±0.10

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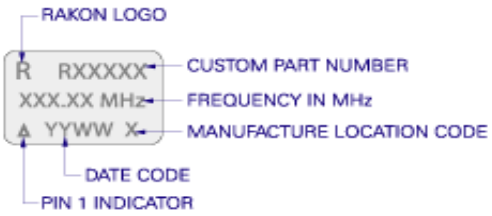
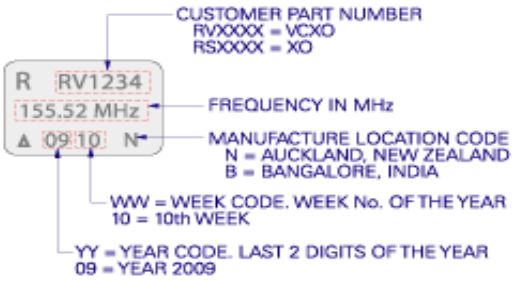
VCXO / XO7500 LID MARKING



LASER MARKING EXAMPLE



TITLE: VCXO7500 SERIES LID MARKING	FILENAME: CAT089	Tolerance:	
RELATED DRAWINGS:	REVISION: A1	XX	±0.5
PRELIMINARY	DATE: 07-Apr-09	X.X	±0.2
	SCALE: NTS	X.XX	±0.10
	Millimetres [inch]	X.XXX	±0.05
		X°	±1.0°
		Hole	±0.10

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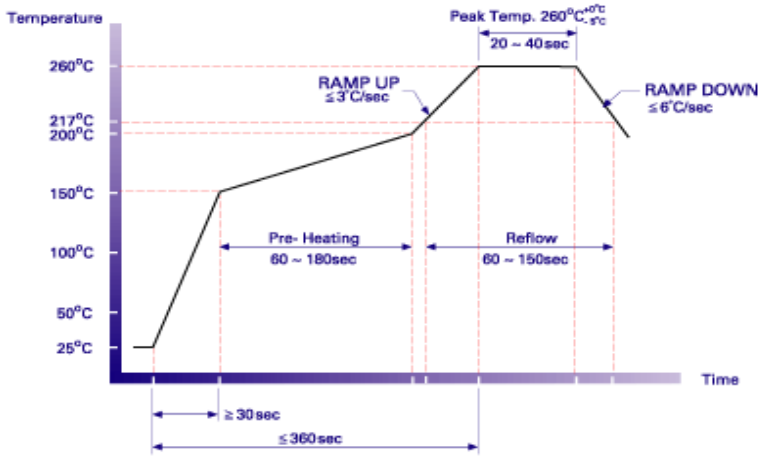

NOTE:

The product has been tested to withstand the Reflow Profile shown. The Reflow Profile used to solder Rakon VCXO/XO is determined by the solder paste manufacturer's specification. It is recommended that the Reflow Profile used does not exceed the one shown above.

TITLE: VCXO7500 SERIES Pb-FREE REFLOW	FILENAME: CAT033	
RELATED DRAWINGS:	REVISION: A	
	DATE: 30-Mar-09	
	SCALE: NTS	
	Millimetres [inch]	

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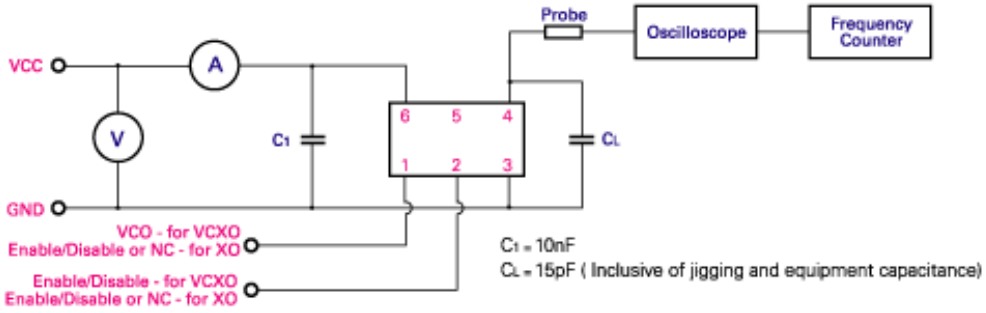
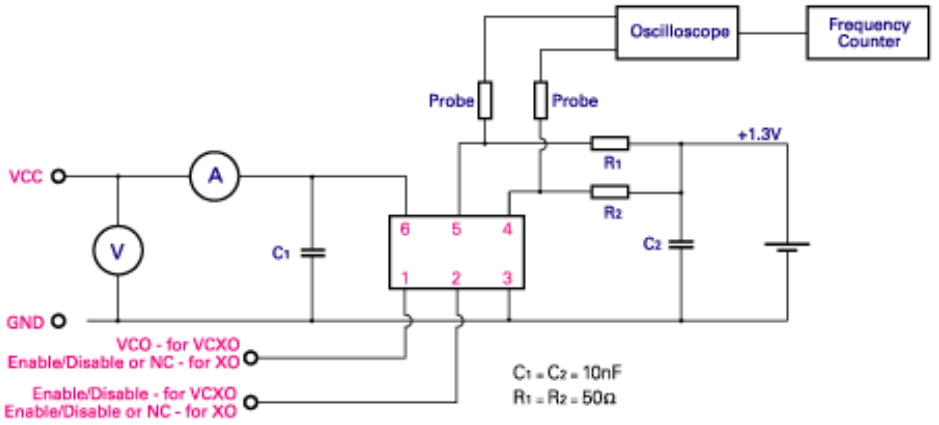
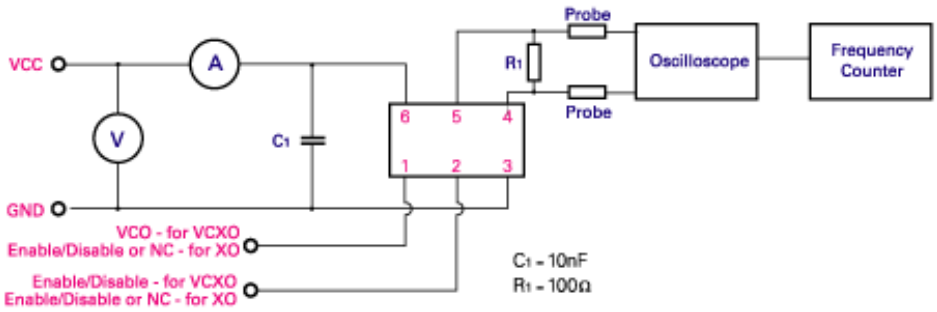
LVCMOS TEST CIRCUIT :



LVPECL TEST CIRCUIT :

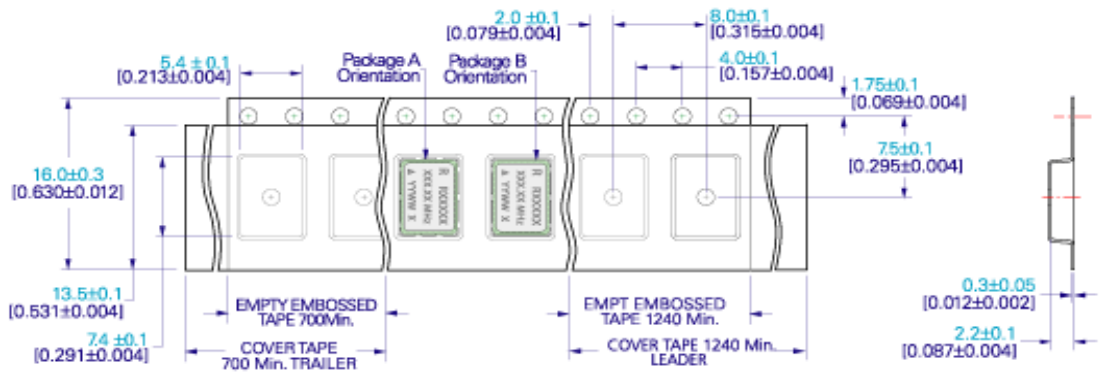


LVDS TEST CIRCUIT :

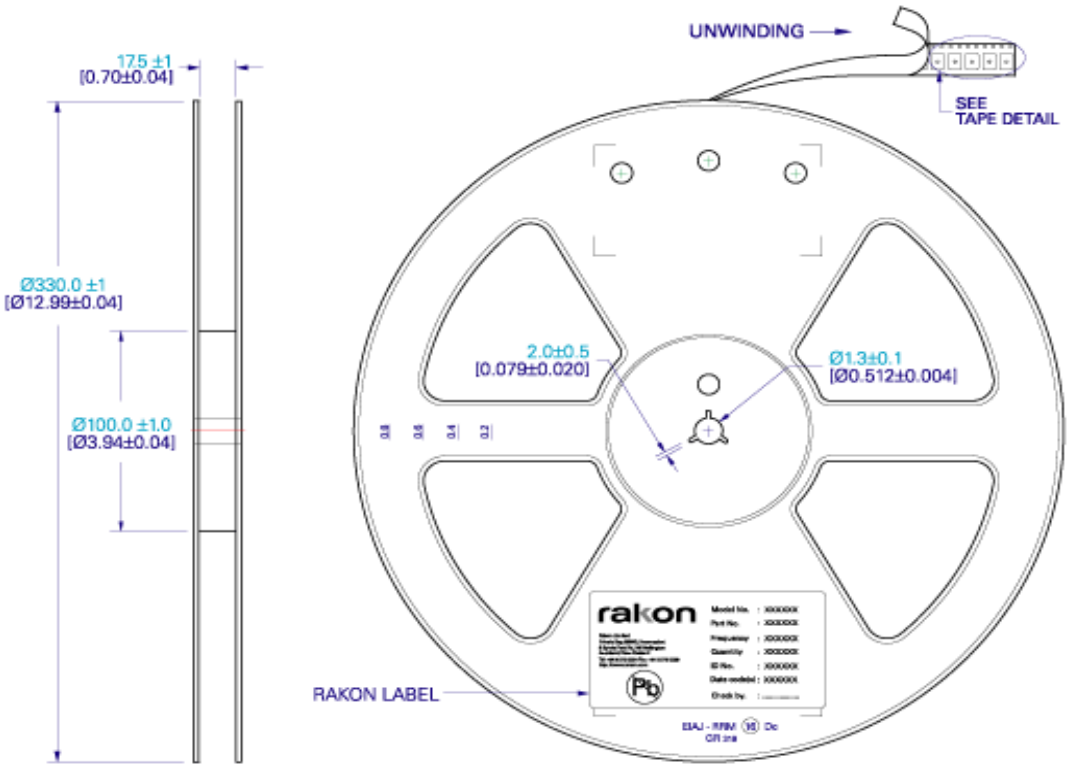


TITLE: VCXO7500 SERIES TEST CIRCUIT		FILENAME: CAT088
RELATED DRAWINGS:	PRELIMINARY	REVISION: A
		DATE: 03-Apr-09
		SCALE: NTS
		Millimetres [inch]

TAPE DETAIL (SCALE 2 : 1)



REEL DETAIL (SCALE 1 : 5)



NOTE: Ø330mm REEL'S STANDARD PACKING QUANTITY IS 2000 OSCILLATORS PER REEL.

TITLE: VCXO7500 Pb-free TAPE & REEL	FILENAME: CAT032	Tolerance:
RELATED DRAWINGS:	REVISION: A	XX =±0.5
	DATE: 30-Mar-09	X.X =±0.2
	SCALE: See above	X.XX =±0.10
	Millimetres [inch]	X.XXX =±0.05
		X° =±1.0°
		Hole =±0.10

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