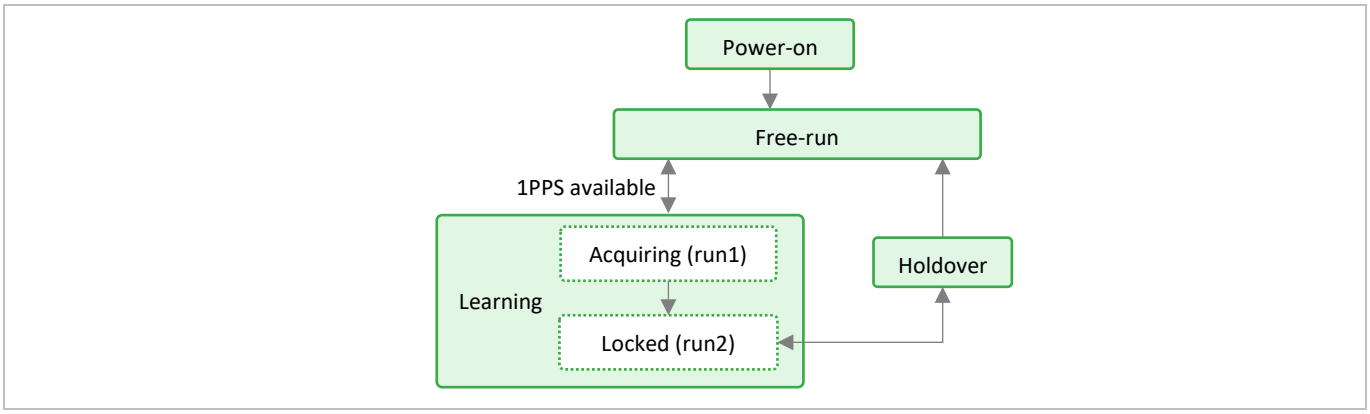
ROD2522S2

The ROD2522S2 is a PPS Disciplined Oscillator (PPSDO) that synchronises its 1PPS and output clock to a specified 1PPS input signal from the GNSS system or the synchronization system output. It is a 0.5 ppb pk-pk PPSDO designed for telecommunications, GNSS modules, and test equipment. The PPSDO begins applying ageing compensation upon signal acquisition, and frequency stability is guaranteed only in locked mode.

Synchronisation occurs during the acquiring phase (run1) and locked phase (run2) when the 1PPS input signal is available. Run1 and run2 together are also defined as the 'Learning' stage.

After 48 hours in locked mode with a clean reference signal, the device provides a 24-hour holdover within 1.5 µs accuracy at ambient temperature (up to a 4°C variation). The system automatically enters locked mode only when both time and frequency stability are guaranteed. Once a 1PPS signal is detected, the system switches to holdover mode when the 1PPS signal is lost.

Please refer to the working flow process diagram below for details in the 'Device Operating States' section.



Key specifications

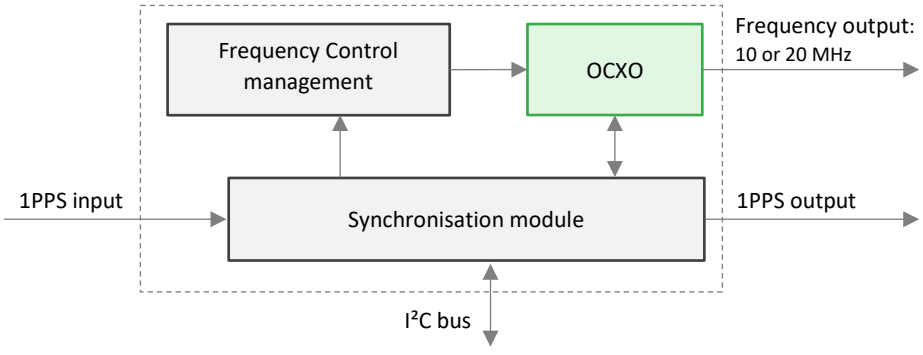
- Frequency (Fn): 10 or 20 MHz
- Holdover: 24-hour (≤1.5 µs, 4°C external temperature variation)
- Frequency stability (FvT): 0.5 ppb pk-pk
- Operating temperature: -40 to 85°C
- Compensated ageing: ±0.02 ppb/day
- Voltage supply: 3.3 V
- I²C bus device status and commands

Applications

- Edge grandmasters
- DU/CU/servers
- Cell-site routers
- Front-haul switches
- NIC time cards
- Test equipment
- GNSS modules

25.4 x 22.0 x 12.1 mm

Block Diagram



ROD2522S2

1.0 Absolute Maximum Rating[1]

Parameter	Min.	Max.	Unit	Note
a. Storage temperature	-40	+85	°C	
b. Supply voltage (V_{CC})	-0.3	3.6	V	
c. Voltage on 1PPS input	-0.3	V_{CC} +0.3	V	
d. Voltage at any digital interface pin with respect to GND	-0.3	V_{CC} +0.3	V	
e. Load for HCMOS RF Output	15	45	pF	
f. Continuous output current for HCMOS RF output		±50	mA	

2.0 Power Supply

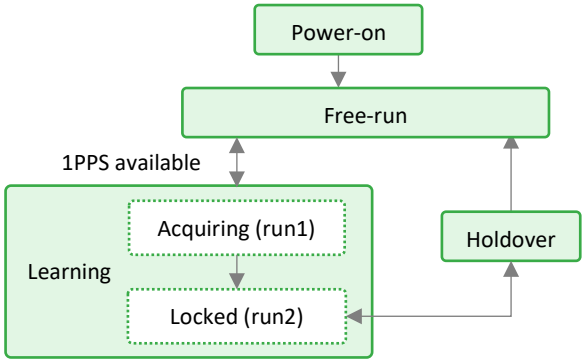
Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Supply voltage (V_{CC})	3.135	3.30	3.465	V	
b. Current consumption			900	mA	During warm-up time
c. Current consumption			300	mA	In steady-state & still air at +25°C
d. Power-on recall voltage	2.2			V	Minimum V_{CC} at which memory recall occurs
e. V_{CC} ramp rate	0.2		100	V/ms	

3.0 RF Signal Output – HCMOS

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Low level output voltage (V_{OL})			0.4	V	
b. High level output voltage (V_{OH})	2.4			V	
c. Rise and fall times			5	ns	from 10% to 90% output levels, 15pF load
d. Duty cycle	45		55	%	At 50% level
e. Load		15	45	pF	
f. Spurious			-80	dBc	
g. Sub-harmonics			-40	dBc	
h. Start-up time			1	Sec	The first valid pulse on the output signal

[1] Operating beyond this limit may result in change or permanent damage to the device.

4.0 Device Operating States



State	Condition/Description
a. Power-on	This state corresponds to the initial operating state of the device. Stabilisation steps and order of magnitude: • Start-up time: 1 second after powering on the device; frequency signal output is delivered (valid clock pulses), within 150 ppm of final frequency. • Power consumption will stabilise within 3 minutes after powering on at +25°C; that stabilisation depends on ambient temperature at the start. The ageing slope will reach its final performance after recovery time (see 'Recovery' specification section)
b. Free-run	1PPS output is not available in the freerun mode The device performs similarly to a stand-alone OCXO delivering its intrinsic performance (no learning or ageing compensation in this state).
c. Acquiring (run1)	When 1PPS become available, the devices transition to acquiring mode and - The state transition happens when the 1PPS signal is present over: • the first 40 seconds and, • 70% minimum of the remaining time, at any point in time; if those conditions are not met, the device returns to free-run mode. 1PPS output is enabled as soon as 4s after the 1PPS input is available. The acquiring state has wide bandwidth on the 1PPS servo. The system prepares for entering the locked mode by initiating the learning mode Once the system is warmed up, phase and frequency are locked within a few minutes (a typical 4 minutes) of a valid 1PPS signal. Cold start requires up to 30 minutes maximum at -40°C). When the acquisition process is successful: • frequency accuracy is guaranteed within less than 1ppb; • phase is aligned to the 1PPS input signal. device transitions to 'locked' mode
d. Locked (run2)	1PPS input available - 1PPS output signal enabled. The loop bandwidth for the 1PPS input signal is optimised. The device delivers the best GNSS stability and OCXO performance. In this state, the device learns ageing information. Phase is locked, frequency is locked & guaranteed.
e. Holdover	From 'locked' mode, if 1PPS input becomes unavailable for a single pulse, then the device goes into 'holdover' mode • Frequency stability over operating temperature is guaranteed. • After initial warm-up, the system requires 2 days of continuous operation to meet specified long holdover stability. • The compensation mechanism continuously corrects the frequency up to half of the cumulated locked time, with a limit of 24 hours. The holdover is guaranteed for 24 hours once there is accumulated learning time of 48 hours. After 24 hours, a constant compensation value is applied to the frequency, and the OCXO module transitions to the 'free run' mode. • The remaining computed holdover duration value can be checked through the OCXO status register (see the Slave Register 0x42 table) In 'holdover' mode, once the 1PPS signal becomes available, the module reverts into 'locked' mode.

5.0 Free-run State

Parameter		Min.	Typ.	Max.	Unit	Test Condition / Description
a. Nominal frequency (Fn)			10, 20		MHz	
b. Frequency calibration (at +25°C ±2°C)				±100	ppb	At time of shipment, reference to nominal frequency [2]
c. 10 years overall stability				±350	ppb	After stabilisation of the device (14 days of continuous operation)
d. Ageing (at shipment/after recovery time)						See 'Recovery' specification section
	per day			±0.2	ppb	Measured before shipment
	per year			±50	ppb	Cumulated (extrapolation)
	10 years			±250	ppb	Cumulated (extrapolation)
e. Frequency stability over operating temperature range				0.5	ppb	Peak-to-peak
f. Hysteresis effect				0.3	ppb	Over -40 to +85°C, gradient 1°C/minute
g. Supply voltage stability				±0.5	ppb	Nominal V_{CC} ± 5% variation
h. Load sensitivity				±0.5	ppb	HCMOS: 15pF to 30pF load variation
i. Acceleration sensitivity				±3	ppb/*g*	Vs. static orientation
j. Warm-up time (to ± 10ppb) at +25°C				3	Minutes	Reference to frequency after 1 hour of continuous operation
k. Retrace vs. operating at ambient				±5	ppb	24h on, 24h off, 1h on
l. SSB phase noise at 10MHz						Static conditions
	1Hz		-100	-90	dBc/Hz	
	10Hz		-130	-120	dBc/Hz	
	100Hz		-145	-140	dBc/Hz	
	1kHz		-150	-145	dBc/Hz	
	10kHz		-155	-150	dBc/Hz	
m. Short term stability (ADEV)						Static conditions
	1s to 100s		3	5	e^{-12}	
	1,000s		3	7	e^{-12}	
	10,000s		10	20	e^{-12}	

[2] The characteristics of the OCXO may be temporarily affected by the processes of assembly, soldering & powered-off time. The frequency specifications apply 48 hours after assembly. Nominal conditions apply unless otherwise stated.

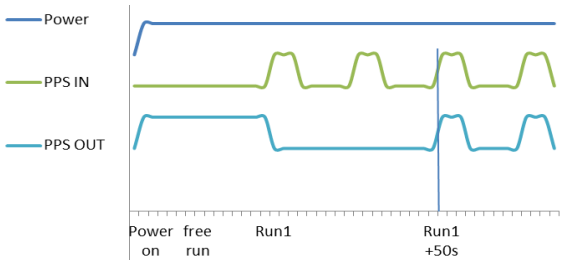
6.0 Acquiring State

Parameter		Min.	Typ.	Max.	Unit	Test Condition / Description
a. Nominal frequency			10, 20		MHz	
b. 1PPS input						
	Waveform compatibility					HCMOS
	Low-level input voltage (V_{IL})	0		1.0	V	
	High-level input voltage (V_{IH})	2.2		V_{CC}	V	
	Pulse width	10		10000	µs	
	Time deviation (TDEV)		20	90	ns	Tau = 100s to 10,000s
c. 1PPS output (available 30s max. after locking on 1PPS input & for 24h in holdover mode)						
	Waveform compatibility					HCMOS
	Low-level input voltage (V_{IL})			0.4	V	Load 15pF // 10kΩ min
	High-level input voltage (V_{IH})	2.4			V	Load 15pF // 10kΩ min
	Pulse width		50		ms	
	Rise and fall time			10	ns	10% to 90% level, 15pF load

Note:

The phase alignment is done on the positive edge of both 1PPS in and out signals.

PSS IN and OUT logic level



7.0 Locked State

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Nominal frequency (Fn)		10, 20		MHz	
b. SSB Phase Noise					Static conditions
1Hz		-100	-90	dBc/Hz	
10Hz		-130	-120	dBc/Hz	
100Hz		-145	-140	dBc/Hz	
1kHz		-150	-145	dBc/Hz	
10kHz		-155	-150	dBc/Hz	
c. Short Term Stability (ADEV)					Static conditions
Tau = 1,000s		6	10	ppt	
Tau = 10,000s		4	7	ppt	
d. 1PPS Input - Waveform compatibility		HCMOS			
Low level input voltage (VIL)	0		1.0	V	
High level input voltage (VIH)	2.2		Vcc	V	
Pulse width	10		10000	µs	
Time deviation (TDEV)					
Tau = 100s to 10,000s		20	90	ns	
e. 1PPS Output – Waveform compatibility		HCMOS			
Low level output voltage (VOL)			0.4	V	Load 15pF // 10kΩ min
High level output voltage (VOH)	2.4			V	Load 15pF // 10kΩ min
Pulse Width		50		ms	
Rise and fall time			10	ns	10% to 90% level, 15pF load
PLL accuracy	-50		50	ns	After 4 hours of disciplining

8.0 Holdover State

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Nominal frequency (Fn)		10, 20		MHz	
b. Frequency stability over -40°C to +85°C			0.5	ppb	Reference to (Fmax - Fmin)
c. Hysteresis effect		0.07	0.2	ppb	Over -40 to +85°C, gradient 1°C/minute
d. Supply voltage stability			±0.5	ppb	Nominal V_{CC} ± 5% variation
e. Load sensitivity			±0.5	ppb	HCMOS: 15pF to 30pF load variation
f. Acceleration sensitivity			±3	ppb/*g*	Vs. static orientation
g. Holdover at 1.5µs (with zero initial frequency and phase error)					
with 4°C variation (symmetrical)	24			hour	With a gradient of 0.5°C/minute
with 10°C variation (asymmetrical)	12				
with 20°C variation (asymmetrical)	4				
h. Supply voltage stability			±0.5	ppb	Nominal VCC ± 5% variation
i. Load sensitivity			±0.5	ppb	HCMOS: 1 to 2 loads (15pF)
j. Acceleration sensitivity			±3	ppb/g	Vs static orientation
k. SSB phase noise at 10 MHz					Static conditions
1Hz offset		-100	-90	dBc/Hz	
10Hz offset		-130	-120	dBc/Hz	
100Hz offset		-145	-140	dBc/Hz	
1kHz offset		-150	-145	dBc/Hz	
10kHz offset		-155	-150	dBc/Hz	
l. Short term stability (ADEV)					Static conditions
Tau = 1s to 1,000s		3	7	e^{-12}	
Tau = 10,000s		6	10	e^{-12}	
m. 1PPS output					Available over 24 hours max. from holdover mode start
Waveform compatibility					HCMOS
Low-level output voltage (V_{OL})			0.4	V	Load 15pF // 10kΩ min
High-level output voltage (V_{OH})	2.4			V	Load 15pF // 10kΩ min
Pulse Width		50		ms	
Rise and fall time			10	ns	10% to 90% level, 15pF load

9.0 I²C Bus Interface

Signal Name	Type	Function	Notes	Logic Levels
a. I²C data	Open drain	Serial data	Min 2kΩ external pull-up resistor, conforms to UM10204 NXP I²C bus specification	2.1V < V_{IH} (High) < 3.3V V_{IL} (Low) < 0.4V
b. I²C clock	Open drain	Serial clock	Min 2kΩ external pull-up resistor, conforms to UM10204 NXP I²C-bus specification	2.1V < V_{IH} (High) < 3.3V V_{IL} (Low) < 0.4V
c. Frequency			100kBit/s min - 400kBit/s max	

Note: At start up, the module performs a self-calibration process after it detects one pulse on 1PPS input. The self-calibration process may last 1 minute maximum. During this time the I²C is not available.

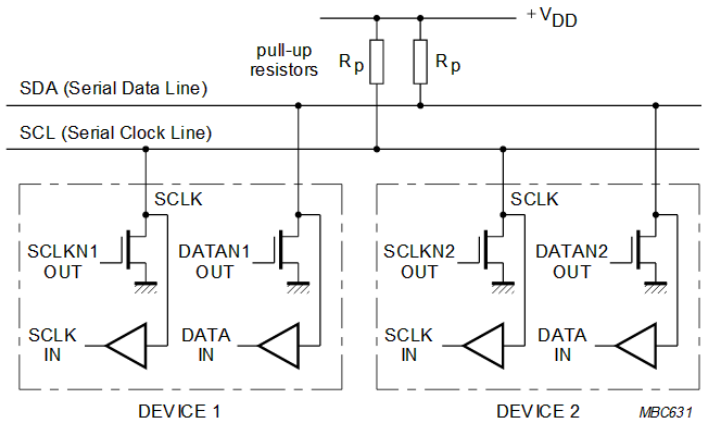
10.0 I²C Communication Conditions

I²C is not able to communicate in full-duplex mode, i.e., TX and RX are mutually exclusive. The Rakon 1PPS Module acts as a slave in the communication setup; therefore, it cannot initiate data transfers on its own. The host, which is always the master, provides the data clock (SCL), and the clock frequency is, therefore, not configurable on the slave.

The I²C module complies with the NXP Inter-IC bus (I²C bus) specification version 2.1. Fast mode up to 400 kbit/s. Fast-mode devices are downwards compatible i.e. they can be used in a 0 to 100 kbit/s Standard I²C bus system.

Only two bus lines and a ground reference are required; a serial data line (SDA) and a serial clock line (SCL). The number of ICs connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

The master must handle the clock stretching feature as stated in the NXP Inter-IC bus (I²C bus) specification version 2.1 as I²C data might be delayed in case of critical timing sensitive computation.

Connection of standard and fast-mode devices to the I²C bus	

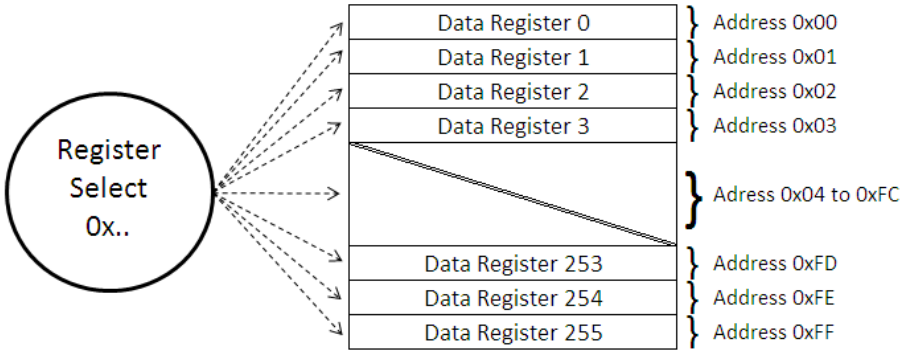
It is generally known that the I²C bus can hang if an I²C master is removed from the bus in the middle of a data read. This can occur because the I²C protocol does not mandate a minimum clock rate. Therefore, if a master is reset in the middle of a read while a slave is driving the data line low, the slave will continue driving the data line low while it waits for the next clock edge.

This prevents bus masters from initiating transfers. If this condition is detected, the following three steps will clear the bus hang condition:

1. An I²C master must generate up to 9 clock cycles.
2. After each clock cycle, the data pin must be observed to determine whether it has gone high while the clock is high.
3. When the data pin is observed high, the master can initiate a start condition.

The receiver's I²C address is set to **0xE0** by default. This address can be changed on request.

The I²C interface allows 256 slave registers to be addressed. As shown in Figure *I²C Register Layout* only a few of these are currently implemented. Others are reserved for future uses or internal computation and must not be addressed.

I²C bus register layout	

Register Detail

The next section contains information about the Rakon module register.

Slave Register:	Refers to the address that has to be sent after the I²C slave address to select the desired register.
Description:	Name and function of the register.
Firmware:	Details on the firmware revision the register is supported on.
Comment:	Additional information regarding the register or the data it represents.
Message Info:	Number of bytes to be read and data type of the data register.

Slave Register	**0x3E**		
Description	Read Temperature Sensor		
Firmware	1.4+		
Comment	Represents an image of the external temperature seen by the module. The value can vary from Ox0000 to Ox0FFF, negative slope		
Message Info	# bytes	Datatype	
	2	U-Short	

Slave Register	**0x41**		
Description	Read Frequency Control		
Firmware	1.4+		
Comment	Range can swing from Ox00000000 to Ox000C8320. 8E-13 typical frequency variation per step		
Message Info	# bytes	Datatype	
	4	U-Long	

Slave Register	**0x42**		
Description	Read Status		
Firmware	1.4+		
Comment	Gives information regarding the state of the module and other parameters. Refer to Figure Status Details for more information.		
Message Info	# bytes	Datatype	
	2	Char	

Slave Register	**0x50**		
Description	Read Product Identification		
Firmware	1.4+		
Comment	Product traceability information ASCII format		
Message Info	# bytes	Datatype	
	64	Char	

Slave Register	**0x51**		
Description	Read firmware revision		
Firmware	1.4+		
Comment	Includes the name, version revision, release date and special parameters. ASCII format		
Message Info	# bytes	Datatype	
	64	Char	

Slave Register	**0x52**		
Description	Read Relative Time Interval Error		
Firmware	1.4+		
Comment	Time Interval Error in nanosecond with an offset of +2000ns. Only available when system is locked and phase measurement is available. When there is no 1PPS measurement, system phase equivalent ageing is displayed. Ox0000 to Ox0FFF		
Message Info	# bytes	Datatype	
	2	U-Short	

Slave Register	**0x60**		
Description	Read Real Time Clock Calendar		
Firmware	2.5+		
Comment	Encoded in BCD (binary coded decimal) format. Hours - Minutes - Seconds - Years - Months - Days - WeekDay Example : 0x010002030201020500020200 04 Thursday 20 February 2025 10:23:21		
Message Info	# bytes	Datatype	
	13	BCD	

Slave Register	**0x0D**	
Description	Read Manual Phase offset compensation.	
Firmware	2.5+	
Comment	Read the custom phase offset delay compensation. First byte will always be 0, offset of +127. Example : 0x008A for +11 nanoseconds or 0x0038 for -71 nanoseconds.	
Message Info	# bytes	Datatype
	2	Byte

Status Detail

The status channel is a bitfield, as shown below:

Byte MSB								Byte LSB						
0	0	0	0	0	0	0	0	**0**	/P.Out	Syst.F	**1**	HV	Lock Status	IsPPS

MSB byte is always 0x00

0	It must be 0 for normal operation.
/P.Out	0: 1PPS ready and available on 1PPS_Out Pin 1: 1PPS not ready and not available on 1PPS_Out Pin D.
Syst.F	System Fail check. If 1PPS has been provided.
1	It must be 1 for normal operation.
HV	1: System in Holdover state 0: System is out of Holdover state, 1PPS detected
Device Status	b00 : Free run b01 : Acquiring (run1) b10 : Locked (run2)
Is1PPS	0: There is no valid 1PPS input available 1: There is a valid 1PPS input

Write Access

Slave Register	**0x61**		
Description	Write Real Time Clock Calendar		
Firmware	2.5+		
Comment	Encoded in standard hexadecimal. Can only be settled while the PPS is available. Hours - Minutes - Seconds - Years - Months - Days - WeekDay(from 0 to 6) Example : 0x0A162019021404 Thursday 20 February 2025 10:22:32		
Message Info	# bytes	Datatype	
	7	Char	

Slave Register	**0x0C**		
Description	Set Manual Phase offset compensation.		
Firmware	2.5+		
Comment	Compensate a phase offset beetween the PPS Input and Output. The offset is filtered by the main loop. No phase jump will be observed. Can take several hours to compensate the phase. Format is 127 ± X nanoseconds.		
Message Info	# bytes	# bytes	
	1	Byte	

11.0 Marking

Parameter	Test Condition / Description
a. Type	Label
b. Line 1	[Manufacturer identifier] RAKON
c. Line 2	[Part Number][3] SPT####LF
d. Line 3	[Nominal Frequency] E.g., 20MHz
e. Line 4	[Serial Number] 1 Letter + 5 Numerals - SN: L12345 | Batch info
f. Line 5	[Manufacturing Date Code] 4 digits for Year & Week code - DC: YyWw
QR code	[QR code] Batch information 

12.0 Environmental Specification

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Operating temperature range	-40		+85	°C	Temperature gradient ≤ ± 0.5°C/minute, airflow speed between 1m/s and 3 m/s
b. Relative Humidity	5		95	%	
c. Air Pressure	70		106	kPa	

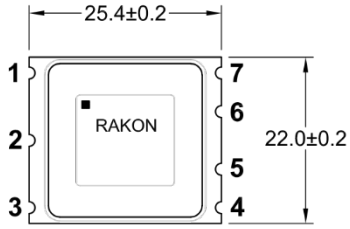
[3] Part Number Convention

13.0 Quality and Reliability Requirements[4]

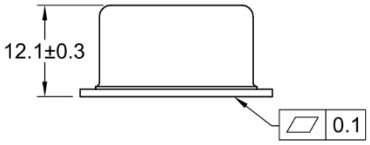
Parameter	Test Condition / Description
a. RoHS compliant	Parts are fully compliant with the European Union directives 2011/65/EU and 2015/863/EU (amending annex II to directive 2011/65/EU) on the restriction of the use of certain hazardous substances in electrical and electronic equipment
b. Solderability	JESD22-B102. Method 2, precondition 150°C, 16 hours
c. Latch up	EIA/JESD78, tested at room temperature and maximum ambient operating temperature
d. Electrostatic discharge (ESD)	Human Body Model (HBM), JS-001-2012, ≥ 2000V Charged Device Model (CDM), JS-002-2022, corner pins ≥ 1000V, middle pins ≥ 500V
e. High temperature storage	JESD22-A103, 1000 hours at 150°C, unbiased
f. Low temperature storage	JESD22-A119, 1000 hours at -55°C, unbiased
g. Thermal shock	MIL-STD-883 Method 1011, 15 cycles from -55°C to 125°C
h. Temperature humidity bias	EIA/JESD22-A101, +85°C / 85% RH, 1008 hours, at max. Vcc
i. Temperature cycling	JESD22-A104, 1000 cycles, -55°C to +125°C, non-operating, 5 to 10 minutes soak
j. High temperature operating life	JESD22-A108D, +125°C, 1008 hours, at max. Vcc
k. Monitored ageing	MIL-PRF-55310F, 1000 hours at +85°C
l. Mechanical shock	JESD22-B-104, 1500*g* peak, 0.5ms pulse duration, 5 pulses in each of 6 directions
m. Mechanical vibration	JESD22-B-103, 20*g* peak acceleration, 10-2000Hz, 4 minutes sweep, 4 sweeps x 3 axes
n. Moisture Sensitivity Level	MSL-3

[4] Qualification, not operational

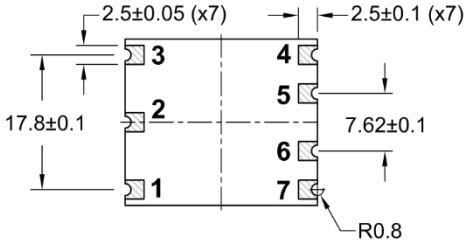
14.0 Model Outline



TOP VIEW



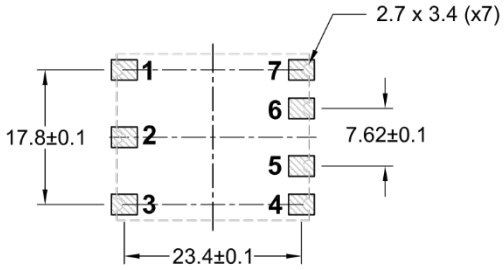
FRONT VIEW



BOTTOM VIEW

RECOMMENDED PAD LAYOUT

- TOP VIEW



NOTE

- Planarity of the bottom PCB ≤0.15mm typicao ≤0.1mm / PCB interfacing with customer's board
- No via, no trace on bottom side
- Unit: mm. Tolerance is ±0.2 mm if it has not been indicated.

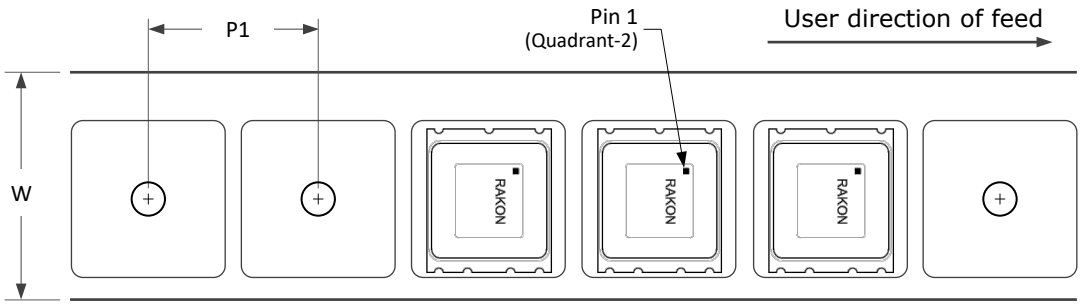
Pin	Connections
1	1PPS Input
2	PPS Output
3	Supply Voltage (V_{CC})
4	RF Output (HCMOS)
5	I^2C Bus – SCL
6	I^2C Bus – SDA
7	GND (mechanical & electrical)

15.0 3D Model

Parameter	Remarks
Package size	25.4 x 22.0 x 12.1 mm
Net weight	11 g/pc
STEP file	ROD2522S2 7-pad 3D model *To open or view the STP file, you will need to import it into one of the following software programs: Autodesk Fusion 360, CATIA, SolidWorks, Solid Edge, TurboCAD, Kubotek KeyCreator, FreeCAD, ABViewer, ShareCAD, or eMachineShop.*

16.0 Tape and Reel

Tape and reel packaging: compliant with Standard EIA-481

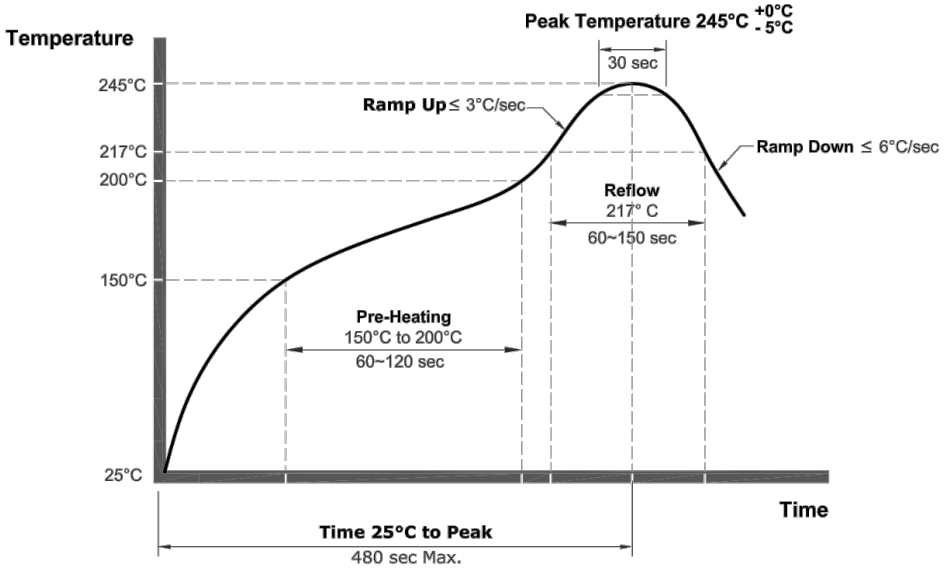


P1	W	SPQ/reel	Reel diameter	Pin 1 orientation
28 mm	44 mm	100pcs. min. 200pcs. max	Φ380 mm	Quadrant-2

17.0 Recommended Reflow Profile

Reflow profile according IPC/JEDEC J-STD-020 with classification temperature Tc 245°C.

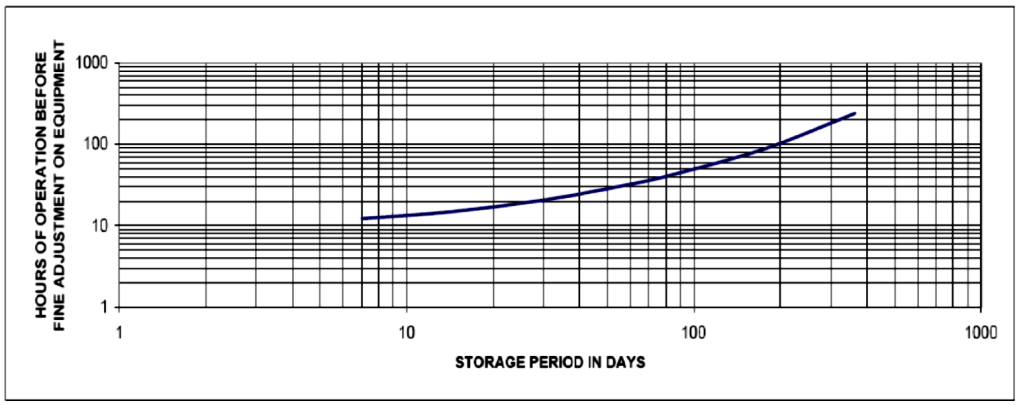
- This product is specifically designed for pick and place reflow manufacturing process.
- The Oscillator must be always on top side during the reflow process.
- The product might be damaged or destroyed when processed top down during second reflow process.



18.0 Recovery

The stability performances of the device are measured before shipment. Then parts are shipped and could remain powered-off for an uncontrolled time, then assembled and tested over the integration process.

Parts could again remain powered off until final installation in the application when they will operate in a continuous mode.

The graph on the right shows the typical recovery time as a function of the unpowered time:	

19.0 Disclaimer

Parameter	Test Condition / Description
a. Disclaimer	"Samples supplied according to this specification are supplied from our development or pre-production programme and are not qualification approved products. No condition, warranty or representation regarding quality, suitability, performance, life or continuation of supply is given or implied, and the Warranty in clause 7 of our standard Conditions of Sale is not applicable. The right is reserved to change the design or specification or cease supply without notice." Rakon Limited