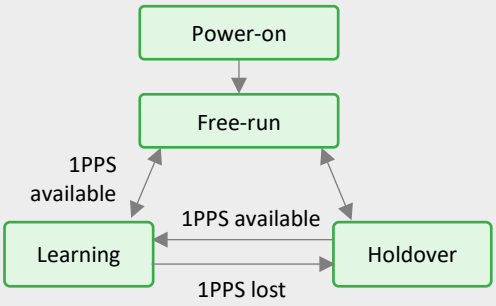
ROD2522S2H

The ROD2522S2H is a PPS Disciplined Oscillator (PPSDO) that synchronizes its 1PPS and output clock to a specified 1PPS input signal from the GNSS system or the synchronization system output. The 0.5 ppb stability PPSDO achieves a 24-hour holdover within ≤1.5 µs accuracy at ambient temperature (up to a 4°C variation). Its compensated ageing is as low as ±0.004 ppb/day, enabling reliable holdover performance. This advanced PPSDO is designed for telecommunications, GNSS modules, and test equipment.

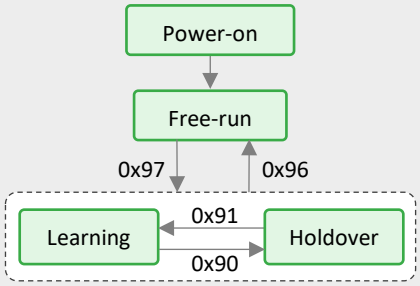
When the 1pps input signal is available, the oscillator is in its 'Learning' stage. Operating in standard mode with the primary reference traceable clock input, the device adapts and understands its ageing behaviour. Once a 1PPS signal is detected, the system switches to holdover mode when 1PPS signals get lost.

Please refer to the working flow process diagram in the 'Device Operating States' section for details.

Automatic State Diagram



Manual Register Driven State Diagram



Key specifications

- Frequency (Fn): 10, 10.24, 12.8 or 20 MHz
- Holdover: 24-hour (≤1.5 µs, 4°C external temperature variation)
- Frequency stability (FvT): 0.5 ppb pk-pk
- Operating temperature: -40 to 85°C
- Compensated ageing: ±0.004 ppb/day
- Free running output: Squarewave with ageing compensation in holdover mode
- Voltage supply: 3.3 V
- I²C bus device status and commands

Applications

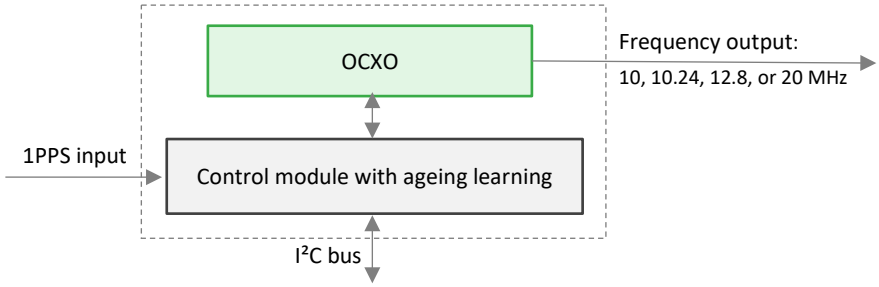
- Edge grandmasters
- DU/CU/servers
- Cell-site routers
- Front-haul switches
- NIC time cards
- Test equipment
- GNSS modules

25.4 x 22.0 x 12.1 mm

Pb FREE

RoHS COMPLIANT

Block daagram



ROD2522S2H

1.0 Absolute Maximum Rating[1]

Parameter	Min.	Max.	Unit	Note
a. Storage temperature	-40	+85	°C	
b. Supply voltage (V_{CC})	-0.3	3.6	V	
c. Voltage on PPS input	-0.3	V_{CC} +0.3	V	
d. Voltage at any digital interface pin with respect to GND	-0.3	V_{CC} +0.3	V	
e. Load for HCMOS RF Output		45	pF	
f. Continuous output current for HCMOS RF output		±50	mA	

2.0 Power Supply

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Supply voltage (V_{CC})	3.135	3.30	3.465	V	
b. Current consumption			900	mA	During warm-up time
c. Current consumption			300	mA	In steady-state & still air at +25°C
d. Power-on recall voltage	2.2			V	Minimum V_{CC} at which memory recall occurs
e. V_{CC} ramp rate	0.2		100	V/ms	

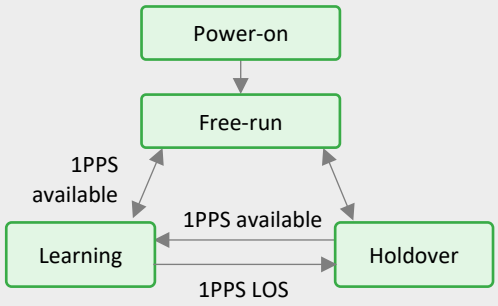
3.0 RF Signal Output – HCMOS

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Low level output voltage (V_{OL})			0.4	V	
b. High level output voltage (V_{OH})	2.4			V	
c. Rise and fall times			5	ns	from 10% to 90% output levels, 15pF load
d. Duty cycle	45		55	%	At 50% level
e. Load		15	45	pF	
f. Spurious			-80	dBc	
g. Sub-harmonics			-40	dBc	
h. Start-up time			1	Sec	

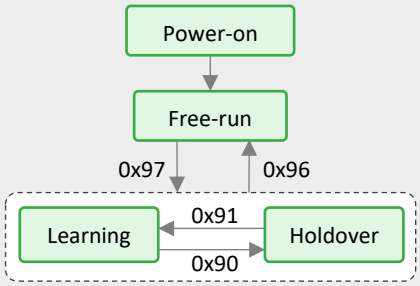
[1] Operating beyond this limit may result in change or permanent damage to the device.

4.0 Device Operating States

Automatic State Diagram



Manual Register Driven State Diagram



State	Condition/Description	Remarks
a. Power-on	This state corresponds to the initial operating state of the device. Stabilisation steps and order of magnitude: - Start-up time: 1 second after powering on the device; frequency signal output is delivered (valid clock pulses), within 150 ppm of final frequency. - Power consumption will stabilise within 3 minutes after powering on at +25°C; that stabilisation depends on ambient temperature at the start. - The ageing slope will reach its final performance after recovery time (see 'Recovery' specification section)	Free-running
b. Free-run	No 1PPS input is available. Similar to a stand-alone OCXO delivering its intrinsic performances (no ageing compensation in this state).	Free-running
c. Learning	1pps input must be available to initiate the Learning state (OCXO ageing data) The duration of the Learning state should be at least twice that of the holdover period targeted.	Free-running
d. Holdover	The device goes into the Holdover state when 1PPS input is unavailable after the Learning state. This state can also be forced through the I^2C command • Frequency stability over operating temperature is guaranteed. • After initial power-on, the system requires 3 days of continuous operation to meet specified holdover stability. • The ageing compensation mechanism continuously corrects the frequency up to half of the cumulated locked time, with a limit of 24 hours. • In the holdover state, if the 1PPS signal becomes available again, the module will revert to the learning state.	Ageing compensation applied

5.0 Free-run States

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Nominal frequency (Fn)		10, 10.24, 12.8, 20		MHz	
b. Frequency calibration (at +25°C ±2°C)			±150	ppb	At the time of shipment, reference to nominal frequency [2]
c. 10 years overall stability			±350	ppb	After stabilisation of the device (14 days of continuous operation)
d. Ageing (at shipment/after recovery time)					See § Recovery
per day			±0.2	ppb	Measured before shipment
per year			±50	ppb	Cumulated (extrapolation)
10 years			±200	ppb	Cumulated (extrapolation)
e. Frequency stability over -40°C to +85°C			0.5	ppb	Peak-to-peak
f. Hysteresis effect		0.07	0.2	ppb	Over -40 to +85°C, gradient 1°C/minute
g. Supply voltage stability			±0.5	ppb	Nominal V_{CC} ± 5% variation
h. Load sensitivity			±0.5	ppb	HCMOS: 15pF to 30pF load variation
i. Acceleration sensitivity			±3	ppb/*g*	Vs. static orientation
j. Warm-up time (to ± 10ppb) at +25°C			3	Minutes	Reference to frequency after 1 hour of continuous operation
k. Retrace vs. operating at ambient			±5	ppb	24h on, 24h off, 1h on
l. SSB phase noise at 10MHz					Static conditions
1Hz offset		-100	-90	dBc/Hz	
10Hz offset		-130	-120	dBc/Hz	
100Hz offset		-145	-140	dBc/Hz	
1kHz offset		-150	-145	dBc/Hz	
10kHz offset		-155	-150	dBc/Hz	
m. Short term stability (ADEV)					Static conditions
1s to 100s		3	5	ppt	
1,000s		3	7	ppt	
10,000s		10	20	ppt	

[2] The characteristics of the OCXO may be temporarily affected by the processes of assembly, soldering & powered-off time. The frequency specifications apply 48 hours after assembly. Nominal conditions apply unless otherwise stated.

6.0 Learning State

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Nominal frequency		10, 10.24, 12.8, 20		MHz	
b. OCXO parameters – see Free-run State section					
c. SSB phase noise at 10MHz					Static conditions
1Hz offset		-100	-90	dBc/Hz	
10Hz offset		-130	-120	dBc/Hz	
100Hz offset		-145	-140	dBc/Hz	
1kHz offset		-150	-145	dBc/Hz	
10kHz offset		-155	-150	dBc/Hz	
d. Short term stability (ADEV)					Static conditions
1s to 100s			3 to 5	ppt	
1,000s			3 to 7	ppt	
10,000s			10 to 20	ppt	
e. 1PPS input					
Waveform compatibility					HCMOS
Low-level input voltage (V_{IL})	0		1.0	V	
High-level input voltage (V_{IH})	2.2		V_{CC}	V	
Pulse width	10		10000	µs	
Time deviation (TDEV)		20	90	ns	Tau = 100s to 10,000s

7.0 Holdover State

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Nominal frequency		10, 10.24, 12.8, 20		MHz	
b. Compensated ageing		±0.004		ppb/day	After a cumulative learning of 48h
c. Frequency stability over over -40°C to +85°C			0.5	ppb	Peak-to-peak
d. Hysteresis effect		0.07	0.2	ppb	Over -40 to +85°C, gradient 1°C/minute
e. Supply voltage stability			±0.5	ppb	Nominal V_{CC} ± 5% variation
f. Load sensitivity			±0.5	ppb	HCMOS: 15pF to 30pF load variation
g. Acceleration sensitivity			±3	ppb/*g*	Vs. static orientation
h. Holdover at 1.5µs (with zero initial frequency and phase error)					
with 4°C variation (symmetrical) with 10°C variation (asymmetrical) with 20°C variation (asymmetrical)	24 12 4			hour	With a gradient of 0.5°C/minute)

8.0 I²C Bus Interface

Signal Name	Type	Function	Notes	Logic Levels
a. I²C data	Open drain	Serial data	Min 2kΩ external pull-up resistor, conforms to UM10204 NXP I²C bus specification	2.1V < V_{IH} (High) < 3.3V V_{IL} (Low) < 0.4V
b. I²C clock	Open drain	Serial clock	Min 2kΩ external pull-up resistor, conforms to UM10204 NXP I²C-bus specification	2.1V < V_{IH} (High) < 3.3V V_{IL} (Low) < 0.4V
c. Frequency			100kBit/s min - 400kBit/s max	

Note: At start up, the module performs a self-calibration process after it detects one pulse on 1PPS input. The self-calibration process may last 1 minute maximum. During this time the I²C is not available.

9.0 I²C Communication Conditions

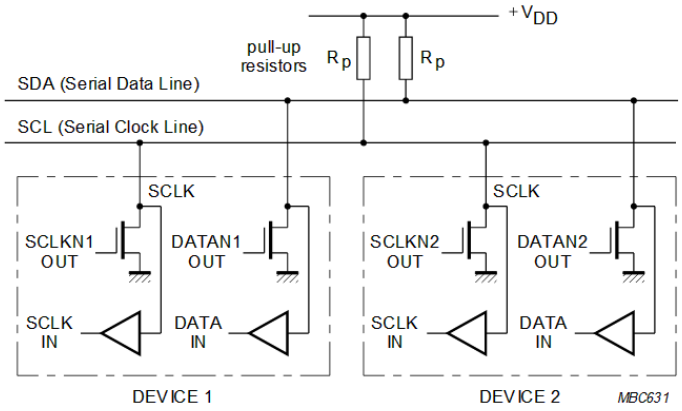
I²C is not able to communicate in full-duplex mode, i.e. TX and RX are mutually exclusive. Rakon PPS Module acts as a slave in the communication setup, therefore they cannot initiate data transfers on their own. The host, which is always the master, provides the data clock (SCL), and the clock frequency is therefore not configurable on the slave.

The I²C module is compliant with the NXP Inter-IC bus (I²C bus) specification version 2.1. Fast mode up to 400 kbit/s. Fast-mode devices are downwards compatible i.e. they can be used in a 0 to 100 kbit/s Standard I²C bus system.

Only two bus lines and a ground reference are required; a serial data line (SDA) and a serial clock line (SCL). The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

The master must handle the clock stretching feature as stated in the NXP Inter-IC bus (I²C bus) specification version 2.1, as I²C data might be delayed in case of critical timing-sensitive computation.

Connection of standard and fast-mode devices to the I²C bus



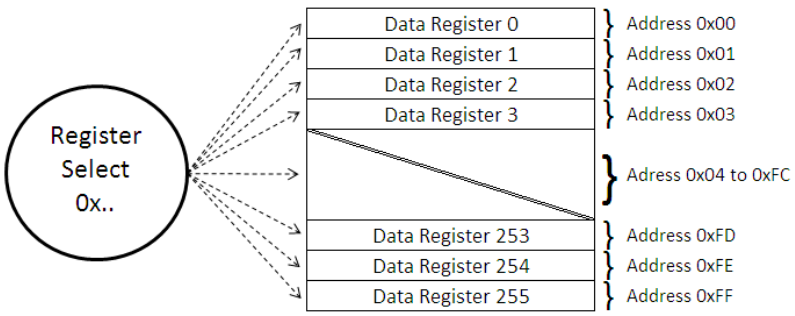
It is generally known that the I²C bus can hang if an I²C master is removed from the bus in the middle of a data read. This can occur because the I²C protocol does not mandate a minimum clock rate. Therefore, if a master is reset in the middle of a read while a slave is driving the data line low, the slave will continue driving the data line low while it waits for the next clock edge.

This prevents bus masters from initiating transfers. If this condition is detected, the following three steps will clear the bus hang condition:

1. An I²C master must generate up to 9 clock cycles.
2. After each clock cycle, the data pin must be observed to determine whether it has gone high while the clock is high.
3. As soon as the data pin is observed high, the master can initiate a start condition.

The receiver's I²C address is set to **0xE0** by default. This address can be changed on request.

The I²C interface allows 256 slave registers to be addressed. As shown in Figure *I²C Register Layout* only a few of these are currently implemented. Others are reserved for future uses or internal computation and must not be addressed.

I²C bus register layout	

Register Detail

The next section contains information about the Rakon module register.

Slave Register:	Refers to the address that has to be sent after the I²C slave address to select the desired register.
Description:	Name and function of the register.
Firmware:	Details on the firmware revision the register is supported on.
Comment:	Additional information regarding the register or the data it represents.
Message Info:	Number of bytes to be read and data type of the data register.

Slave Register	**0x3E**		
Description	Read Temperature Sensor		
Firmware	1.4+		
Comment	Represents an image of the external temperature seen by the module. The value can vary from Ox0000 to Ox0FFF, negative slope		
Message Info	# bytes	Datatype	
	2	U-Short	

Slave Register	**0x41**		
Description	Read Frequency Control		
Firmware	1.4+		
Comment	Range can swing from Ox00000000 to Ox000C8320. 8E-13 typical frequency variation per step		
Message Info	# bytes	Datatype	
	4	U-Long	

Slave Register	**0x42**		
Description	Read Status		
Firmware	1.4+		
Comment	Gives information regarding the state of the module and other parameters. Refer to Figure Status Details for more informations.		
Message Info	# bytes	Datatype	
	2	Char	

Slave Register	**0x50**		
Description	Read Product Identification		
Firmware	1.4+		
Comment	Product traceability information ASCII format		
Message Info	# bytes	Datatype	
	64	Char	

Slave Register	**0x51**		
Description	Read firmware revision		
Firmware	1.4+		
Comment	Includes the name, version revision, release date and special parameters. ASCII format		
Message Info	# bytes	Datatype	
	64	Char	

Slave Register	**0x92**	
Description	Read holdover override status	
Firmware	1.4+	
Comment	Either 0x0000 or 0x0001.	
	If 0 then the system is in holdover even if PPS input is available.	
Message Info	# bytes	Datatype
	2	U-Short

Status Detail

The status channel is a bitfield, as shown below:

Byte MSB								Byte LSB						
0	0	0	0	0	0	0	0	**0**	**x**	Syst.F	**1**	HV	Lock Status	IsPPS

MSB byte is always 0x00

0	Must be 0 for normal operation.			
x	Undefined			
Syst.F	System Fail check. If PPS has been provided.			
1	Must be 1 for normal operation.			
HV	1 : Holdover state, no PPS detected. 0 : not in Holdover state, PPS detected			
Lock Status		**PPS**	**Learning**	**RF Output**
	b00	-	N/A	N/A
	b01	OK	OK	Ageing compensation not available
	b10	OK	OK	Ageing compensation available
IsPPS	Is there a valid PPS input? 0: No / 1: Yes			

Write Access

Slave Register	**0x90**		
Description	Holdover override.		
Firmware	1.4+		
Comment	Force the part to go into holdover even if the PPS signal is present.		
Message Info	# bytes	Datatype	
	none	none	

Slave Register	**0x91**		
Description	Disable the holdover override.		
Firmware	1.4+		
Comment	Force the part to go out of holdover and into free-run state even if the PPS signal is not available.		
Message Info	# bytes	Datatype	
	none	none	

Slave Register	**0x96**		
Description	Disable learning and force Free-run state		
Firmware	1.5+		
Comment	Disable learning feature even if PPS signal is present – Forces the part in Free-run state		
Message Info	# bytes	# bytes	
	none	none	

Slave Register	**0x97**		
Description	Enables learning		
Firmware	1.5+		
Comment	Clears the 'Disable learning' setting (see 0x96) Enables learning feature – Device goes into relevant run state		
Message Info	# bytes	# bytes	
	2	2	

Slave Register	**0x98**		
Description	Clear learning parameters		
Firmware	1.5+		
Comment	Clears all stored learning parameters acquired – once enacted, device would start learning from scratch if feature is enabled. If used in Holdover state, then device would go out of Holdover (to Free-run or Learning state)		
Message Info	# bytes	# bytes	
	2	2	

10.0 Marking

Parameter	Test Condition / Description
a. Type	Label
b. Line 1	[Manufacturer identifier] RAKON
c. Line 2	[Part Number][3] STP####LF
d. Line 3	[Nominal Frequency] E.g., 20MHz
e. Line 4	[Serial Number] 1 Letter + 5 Numerals - SN: L12345 | Batch info
f. Line 5	[Manufacturing Date Code] 4 digits for Year & Week code - DC: YyWw
QR code	[QR code] Batch information 

11.0 Environmental Specification

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
a. Operating temperature	-40		+85	°C	Temperature gradient ≤ ± 0.5°C/minute, airflow speed between 1m/s and 3 m/s
b. Relative humidity	5		95	%	
c. Air Pressure	70		106	kPa	

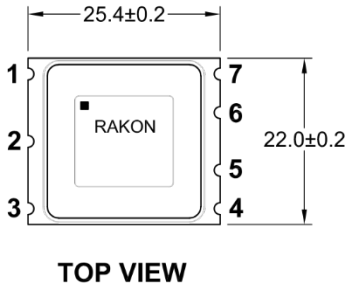
12.0 Quality and Reliability Requirement [4]

Parameter	Test Condition / Description
a. RoHS compliant	Parts are fully compliant with the European Union directives 2011/65/EU and 2015/863/EU (amending annex II to directive 2011/65/EU) on the restriction of the use of certain hazardous substances in electrical and electronic equipment
b. Solderability	JESD22-B102. Method 2, precondition 150°C, 16 hours
c. Latch up	EIA/JESD78, tested at room temperature and maximum ambient operating temperature
d. Electrostatic discharge (ESD)	Human Body Model (HBM), JS-001-2012, ≥ 2000V Charged Device Model (CDM), JS-002-2022, corner pins ≥ 1000V, middle pins ≥ 500V
e. High temperature storage	JESD22-A103, 1000 hours at 150°C, unbiased
f. Low temperature storage	JESD22-A119, 1000 hours at -55°C, unbiased
g. Thermal shock	MIL-STD-883 Method 1011, 15 cycles from -55°C to 125°C
h. Temperature humidity bias	EIA/JESD22-A101, +85°C / 85% RH, 1008 hours, at max. Vcc
i. Temperature cycling	JESD22-A104, 1000 cycles, -55°C to +125°C, non-operating, 5 to 10 minutes soak
j. High temperature operating life	JESD22-A108D, +125°C, 1008 hours, at max. Vcc
k. Monitored ageing	MIL-PRF-55310F, 1000 hours at +85°C
l. Mechanical shock	JESD22-B-104, 1500*g* peak, 0.5ms pulse duration, 5 pulses in each of 6 directions
m. Mechanical vibration	JESD22-B-103, 20*g* peak acceleration, 10-2000Hz, 4 minutes sweep, 4 sweeps x 3 axes
n. Moisture Sensitivity Level	MSL-3

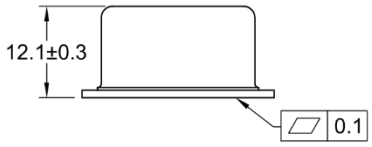
[3] Part Number Convention

[4] Qualification, not operational.

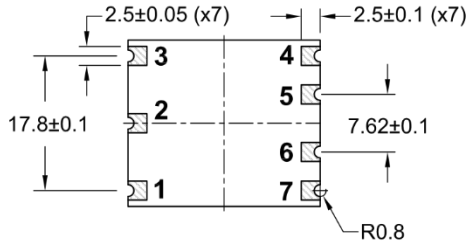
13.0 Model Outline and Pin Connections



TOP VIEW



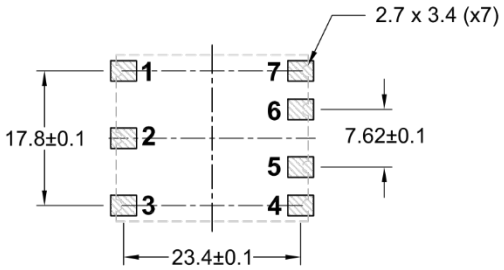
FRONT VIEW



BOTTOM VIEW

RECOMMENDED PAD LAYOUT

- TOP VIEW



NOTE

- Planarity of the bottom PCB ≤0.15mm typicao ≤0.1mm / PCB interfacing with customer's board
- No via, no trace on bottom side
- Unit: mm. Tolerance is ±0.2 mm if it has not been indicated.

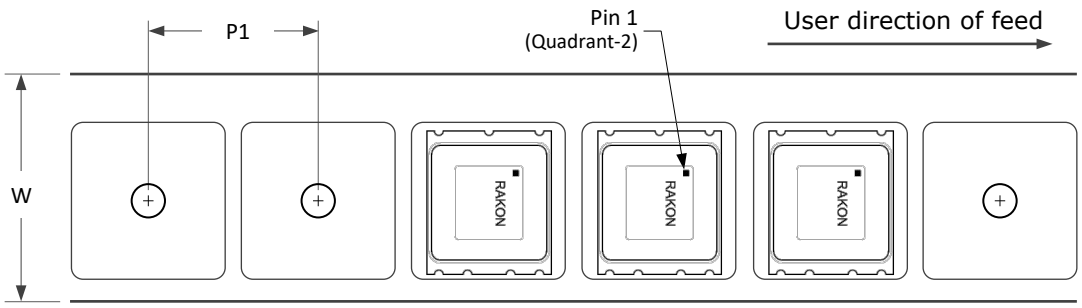
Pin	Connections
1	1PPS Input
2	Do not connect
3	Supply Voltage (V_{CC})
4	RF Output (HCMOS)
5	I^2C bus – SCL
6	I^2C bus – SDA
7	GND (mechanical & electrical)

1.0 3D Model

Parameter	Remarks
Package size	25.4 x 22.0 x 12.1 mm
Net weight	11 g/pc
STEP file	ROD2522S2H 7-pad 3D model *To open or view the STP file, you will need to import it into one of the following software programs:* *Autodesk Fusion 360, CATIA, SolidWorks, Solid Edge, TurboCAD, Kubotek KeyCreator, FreeCAD, ABViewer, ShareCAD, or eMachineShop.*

2.0 Tape and Reel

Tape and reel packaging: compliant with Standard EIA-481

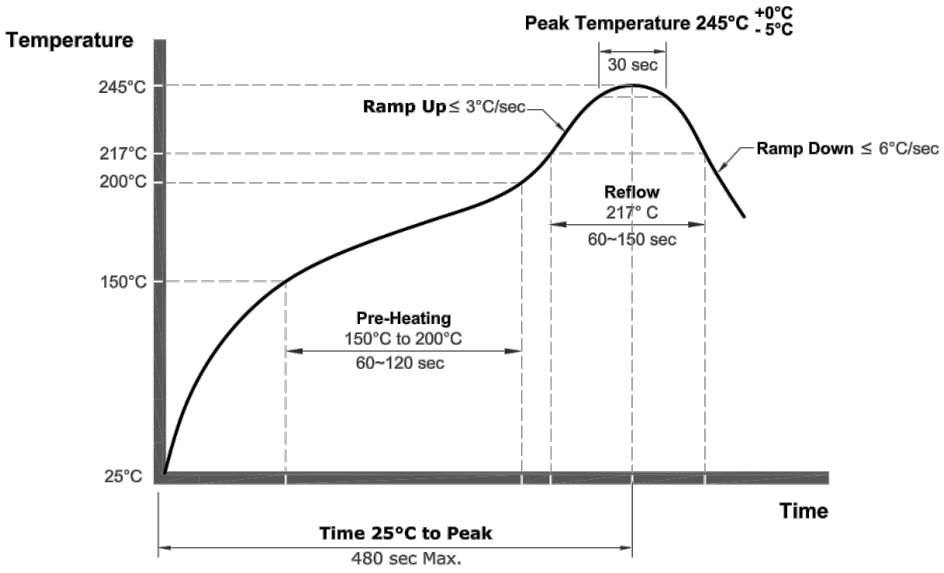


P1	W	SPQ/reel	Reel diameter	Pin 1 orientation
28 mm	44 mm	600 pcs/reel (TBC)	Φ380 mm	Quadrant-2

3.0 Recommended Reflow Profile

Reflow profile according IPC/JEDEC J-STD-020 with classification temperature Tc 245°C.

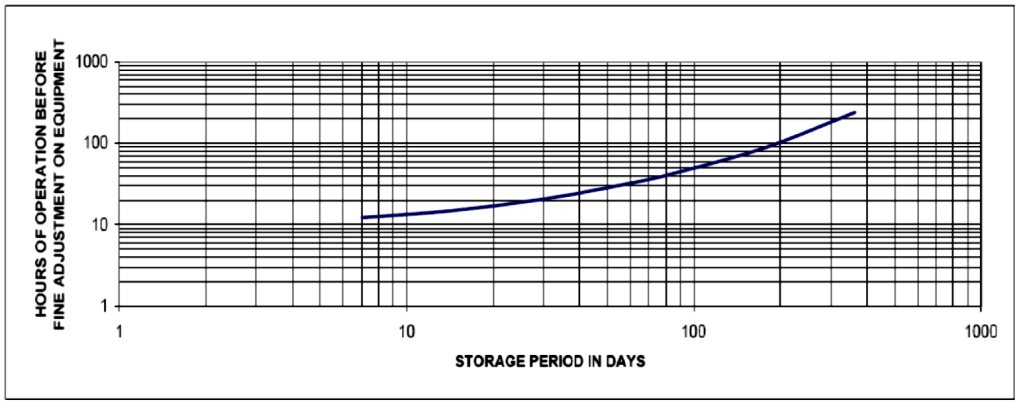
- This product is specifically designed for pick and place reflow manufacturing process.
- The Oscillator must be always on top side during the reflow process.
- The product might be damaged or destroyed when processed top down during second reflow process.



4.0 Recovery

The stability performances of the device are measured before shipment. Then parts are shipped and could remain powered-off for an uncontrolled time, then assembled and tested over the integration process.

Parts could again remain powered off until final installation in the application when they will operate in a continuous mode.

The graph on the right shows the typical recovery time as a function of the unpowered time:	

5.0 Disclaimer

Parameter	Test Condition / Description
a. Disclaimer	"Samples supplied according to this specification are supplied from our development or pre-production programme and are not qualification approved products. No condition, warranty or representation regarding quality, suitability, performance, life or continuation of supply is given or implied and Warranty in clause 7 of our standard Conditions of Sale is not applicable. The right is reserved to change the design or specification or cease supply without notice." Rakon Limited