PLO NS 1PPS [PRELIMINARY]

The PLO NS 1PPS is a part of Rakon's Phase Locked Oscillator (PLO) series with cost-effective and low power consumption. This high reliability 1PPS Space GNSS disciplined oscillator is available at 10 MHz with either square or sinus output waveform options. The filtered 1PPS output signals and <±0.1 ppb overall frequency stability make the product a high-end precision timing PLO.

The 1PPS oscillator is designed for NewSpace smallsats, Low Earth Orbit (LEO) constellations and launchers, where tolerance to Total Ionizing Dose (TID), low power consumption, good phase noise and excellent long term stability are critical requirements. This NewSpace 1PPS PLO supports missions for up to 8 years.

Key Features

- Output frequency: 10 MHz
- Supply voltage: 2 x 12 V
- Stead state consumption: 1.7 W
- Overall frequency stability: <±0.1 ppb

Baseline

- ADEV (1s): <2E-11 @ 10 MHz
- Output wave form: Square and 1PPS
- TID: 30 kRads
- Latch-up free up to LET = 43 MeV/mg/cm^2

Options

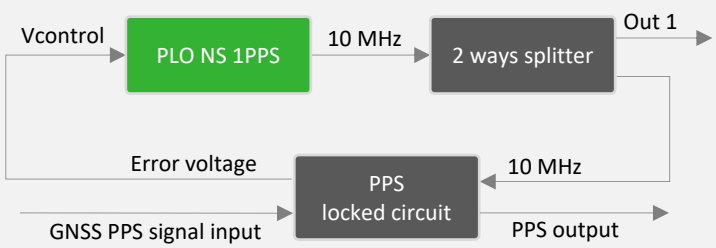
- Clock reference
- Replacement of CSAC
- Position, Navigation and Timing (PNT)

65 x 65 x 30 mm

Image coming soon

Blog Diagram

Application example



Environmental Conditions

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
Operating temperature	TO_P	-20	25	65	°C
Stitch-on temperature	TSo	-40		85	°C
Non-operating temperature	TNOp	-25		85	°C
Random vibration	20 to 50 Hz: +6 dB/oct 50 to 350 Hz: 0.8 g²/Hz 350 to 2000 Hz: -6 dB/oct				
Sine vibration	Level as per MIL-STD-202 Method 204, Condition D (20G)				
Mechanical shock	Level as per MIL-STD-202, Method 213, conduction F: Half sine with a peak acceleration of 1500 *g* for a duration of 0.5 ms				
Radiation	Total Ionizing Dose (TID) of 40 kRad, low dose rate (36 to 360 rad/h) No SEL up to LET = 43 MeV/mg/cm²				
Shocks	Mechanical shock as per MIL-STD-202, Method 213: half sine with a peak acceleration of 1500*g* for a duration of 0.5 ms				
Radiation	Total Ionizing Dose of 30 kRad, low dose rate (36 to 360 rad/h) Latch up free up to LET = 43 MeV.cm².mg^{-1}				

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Process

Parameter	Details
Warm-up	This stage corresponds to the initial operating mode of the device. It could occur after a long power-off time (storage, installation process, etc.). Due to the frequency recovery phenomenon, the device must be re-stabilised over a continuous time of operation before reaching its overall intrinsic performance (up to 10 days maximum after 1 year of storage). Stabilisation steps & order of magnitude: • Start-up time within 1 second after powering on the device; frequency signal output is delivered within ppm of final frequency. • Power consumption will stabilise after a few minutes after powering on at +25°C. This stabilisation is dependent on the ambient temperature at the start (up to 20 minutes maximum at -20°C). • The temperature of the oven of the OCXO will be stabilised within less than 10 minutes at -20°C, but no PPS output is available at that stage. • The ageing slope will reach its final performance after recovery time.
Free run	Featured stand-alone OCXO delivers its intrinsic performances, except ageing slope (as it depends on the recovery phenomenon). System stabilisation process for preparing the data acquisition stage. No 1PPS output.
Important	The oven (power supply N°1) should be kept powered all the time when the system is in OFF configuration (5mn), the µ-controller is in stand-bye and oscillator RF generation is OFF (power supply N°2). The most recent OCXO compensation information will be kept in the µcontroller memory.
Acquiring (Run-1)	• From OFF configuration to ON configuration, the oscillator will be powered and the µ-controller will be operational again. • The most recent compensation information will be used to reach the same frequency value as before to switch OFF the oscillator whether the 1PPS is available or not. • If the 1PPS is available, the performance of the OCXO will be improved and will keep the frequency stability. • If the 1PPS is not available, the system will go in holdover mode.
Functional modes	1PPS input must be available for starting the process; it lasts 30 minutes max. at -20°C after reset. 1PPS signal input must be present over: o The first 40 seconds and, o a minimum of 70% of the remaining time, at any time (if those conditions are not met, then it goes back to free-run mode). 1PPS output is coming into force 50s after the 1PPS input is available. Short time loop. Able to handle system stabilisation. Start computing data for the locked mode. On Hot system (after warm-up time), phase & frequency are tuned within a few minutes, while a Cold start requires more time for the system to be stable enough (up to 30 minutes at -20°C). When the acquisition process is successful (30 min. total time minimum): o Frequency accuracy is guaranteed within less than 1 ppb, o Phase is aligned to the 1pps input signal.
Holdover	After a suitable disciplining sequence, TIE (phase difference between the 1PPS input and output signal) is guaranteed: • 1PPS input signal is not available. • 1PPS output signal is available. Frequency stability over operating temperature is guaranteed. After initial warm-up, the system requires 3 days of continuous operation for meeting specified holdover stability. The Holdover Time (HOT) is guaranteed within half of the cumulated locked time, with a limit of 24 hours after 48 hours of locked mode minimum.

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Free Rum Mode

RF Output	Condition / Remarks	Min.	Typ.	Max.	Unit
Nominal frequency			10		MHz
Frequency calibration	@25°C ±2°C	-50		50	ppb
Ageing	Per day Over 8 years	-1 -300		1 300	ppb
Frequency stability (all conditions)	Temperature, ageing, radiation, supply voltage			600	ppb
Warm-up time @20°C				10	min.
SSB phase noise	@1 Hz offset @10 Hz offset @100 Hz offset @1 kHz offset @10 kHz offset			-85 -115 -135 -150 -155	dBc/Hz

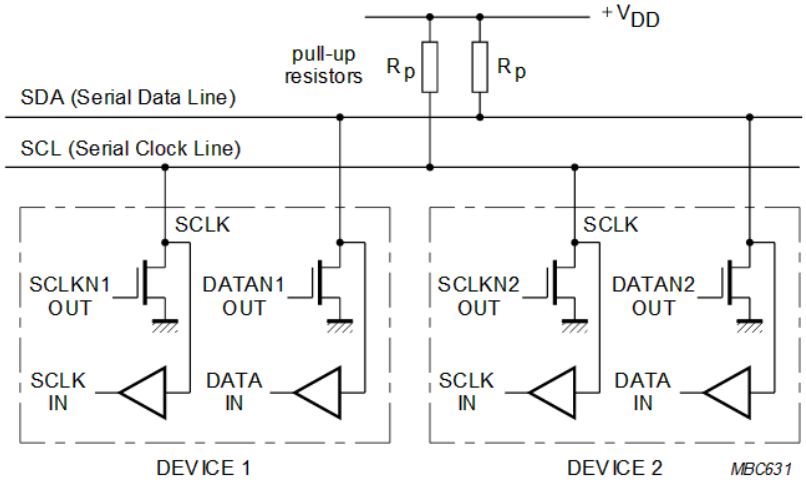
Holdover Mode

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
RF Output					
Frequency			10		MHz
Format			CMOS		
Amplitude		3.00		0.5	V
Load impedance			1 to 3 CMOS gates		
1PPS Output					
Rise/fall time (10% - 90%)	at load capacitance 10 pF			10	ns
Plus width	at load capacitance 10 pF			100	ns
Amplitude		0.50		3	V
Level		0		3.3	V
Logic height (Vch) min.		2.8			V
Logic Low (Vch) max.				0.3	V
Load impedance			1 to 3 CMOS gates		
1PPS Input					
Format			Rising edge		
Low level				0.5	V
High level		2.50		3	V
Load impedance			1		MΩ
Serial Communication					
Protocol			I^2C		
Impedance			Opened collector		
Bit rate	No flow control			100k	Bits/s
Power Input					
Stead	Vacuum @25°C		1.7		W
Warm-up			4	4.5	W
Input voltage		11.4	12	12.6	V

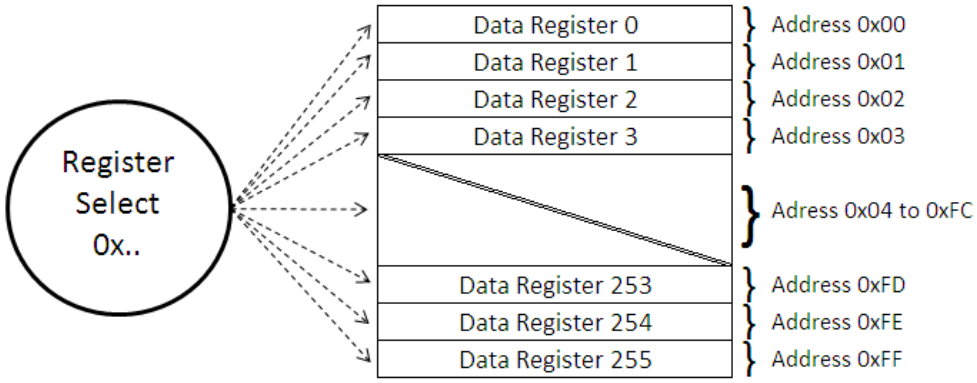
Screening Options

Parameter	Requirement and Condition	EM Options	FM Options
Ageing	@max. operating temperature range	-	✓
Random acceleration	Level as per MIL-STD-202, Method 214, Condition I-D	-	✓
Thermal shocks	MIL-STD-202, Method 107, Condition A1	-	✓
Final measurement	MIL-STD-883, Method 2020, Condition B	✓	✓
External visual inspection	MIL-STD-883, Method 2009	✓	✓

I²C Communication Conditions

Parameter	Details
	I²C is not able to communicate in full-duplex mode, i.e. Tx and Rx [1]are mutually exclusive. Rakon's PPS Module acts as a slave in the communication setup. Therefore they cannot initiate data transfers on their own. The host, which is always master, provides the data clock (SCL), and the clock frequency is therefore not configurable on the slave. The I²C module is compliant with the Philips Semiconductors Inter-IC bus (I²C-bus) specification version 2.1. Fast mode up to 400 kbit/s. Fast-mode devices are downwards compatible, i.e. they can be used in a 0 to 100 kbit/s Standard I²C-bus system. Only two bus lines and a ground reference are required; a serial data line (SDA) and a serial clock line (SCL). The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF. Master must handle clock stretching feature as stated in the Philips Semiconductors Inter-IC bus (I²C-bus) specification version 2.1 as I²C data might be delayed in case of critical timing sensitive computation.
Figure 1: **Connection of Standard and Fast-mode Devices to the I²C-bus**	
	It is generally known that the I²C bus can hang if an I²C master is removed from the bus in the middle of a data read. This can occur because the I²C protocol does not mandate a minimum clock rate. Therefore, if a master is reset in the middle of a read while a slave is driving the data line low, the slave will continue driving the data line low while it waits for the next clock edge. This prevents bus masters from initiating transfers. If this condition is detected, the following three steps will clear the bus hang condition: 1. An I²C master must generate up to 9 clock cycles. 2. After each clock cycle, the data pin must be observed to determine whether it has gone high while the clock is high. 3. As soon as the data pin is observed high, the master can initiate a start condition.

[1] Tx and Rx = Transceiver and Receiver.

	The receiver's I²C address is set to 0xE0 by default. This address can be changed on request. The I²C interface allows 256 slave registers to be addressed. As shown in Figure I²C Register Layout only a few of these are currently implemented. Others are reserved for future uses or internal computation and must not be addressed.
Figure 2: **I²C Register Layout**	
Register detail	Next information will procure details regarding Rakon's module register. Slave Register: Refers to the address that has to be sent after the I²C slave address to select the desired register. • Description: Name and function of the register. • Firmware: Details on the firmware revision the register is supported on. • Comment: Additional information regarding the register or the data it represents. • Message Info: Number of bytes to be read and data type of the data register.

Slave Register	**0x3E – Read Temperature Sensor**		
Firmware	1.4+		
Comment	Represents an image of the external temperature seen by the module. The value can vary from Ox0000 to Ox0FFF, negative slope		
Message Info	# bytes	Data-type	
	2	U-long	

Slave Register	**0x41 – Read Frequency Fontrol**		
Firmware	1.4+		
Comment	The range can swing from Ox00000000 to Ox000F4240. 8E-13 typical frequency variation per step		
Message Info	# bytes	Data-type	
	4	U-long	

Slave Register	**0x42 – Read Status**		
Firmware	1.4+		
Comment	Give information regarding the mode of the module and other parameters. Refer to Figure Status Details for more information. TBD		
Message Info	# bytes	Data-type	
	1	Char	

Slave Register	**0x50 – Read Product Identification**		
Firmware	1.4+		
Comment	Product traceability information ASCII format		
Message Info	# bytes	Data-type	
	64	Char	

Slave Register	**0x51 – Read Firmware Revision**		
Firmware	1.4+		
Comment	Includes the name, version revision, release date and special parameters. ASCII format		
Message Info	# bytes	Data-type	
	64	Char	

Slave Register	**0x52 – Read Relative Time Interval Error (TIE)**		
Firmware	1.4+		
Comment	Time Interval Error in a nanosecond with an offset of +2000 ns. Only available when the system is locked, and phase measurement is available. When there is no PPS measurement, system phase equivalent ageing is displayed. Ox0000 to Ox0FFF		
Message Info	# bytes	Data-type	
	2	U-Short	

Status details

The status channel is bitfield information, as shown below

Byte MSB								Byte LSB						
0	0	0	0	0	0	0	0	0	/P.Out	Syst.F	1	HV	Lock Status	IsPPS

MSB byte is always 0x00

0	Must be 0 for normal operation.
/P.Out	0: PPS ready and available on PPS_Out Pin D. 1: PPS not ready and not available on PPS_Out Pin D.
Syst.F	System Fail check. If PPS has been provided.
1	Must be 1 for normal operation.
HV	1: Holdover Mode, no PPS detected. 0 : not in Holdover mode, PPS detected
Lock Status	b00: System just started (power on mode, free run mode) b01: 30s to 30mn since system started – Stabilization (run1 mode) b10: System ready for use (Run2 mode)
IsPPS	Is there a valid PPS input? 0: No / 1: Yes

Write Access	The receiver does not provide any write access.

Mode Outline and Connectors

Parameter	Condition / Remarks	Connectors
Package type	Pin through-hole Size: 60 x 60 x 30 mm	1PPS signal input SMA
		10 MHz square signal output SMA
		1PPS signal output SMA
		Power supply 1 & 2, ground, serial communication, and pin connections

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