**RHT1490A**

The RHT1490A is a high frequency, low noise TCXO that delivers world class telecommunications grade stability with low RMS phase jitter. This product’s frequency output enables lower system jitter, allowing communication system architects to optimise noise budget and performance. With a frequency stability performance of ±0.25 ppm, its CMOS output generates < 200 fs of RMS phase jitter (for a
98.304 MHz device, bandwidth 12 kHz – 20 MHz). The RHT1490A strikes the optimal balance between close-in phase noise and the noise floor, making it suited to be the single reference clock used for both network and air interface requirements. Its ultra-low noise floor performance helps to achieve very low system clock RMS jitter levels needed in high speed interfaces.

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| Features | Applications  |  | 14.4 x 9.2 x 4.7 mm |
| * Stability as low as ±0.25 ppm
* Low jitter 200 fs (12 kHz to 20 MHz)
* High frequency from 50 – 204.8 MHz
* Patented “Tilt Compensation” to guarantee performance for life of equipment
* Inherent airflow resistance
 | * Sync PLL Embedded Switches
* Designs requiring low noise
* ITU-T G.813 and G.8262
* Low noise C-RAN radios, Microwave links and Small Cells
* Radio head Clock Recovery (IEEE 1588/SyncE)
* 10/25/40G Ethernet
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**Standard Specifications**

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| Parameter  | Min. | Typ. | Max. | Unit | Test Condition / Description  |
| Nominal frequency |  | 50 – 204.8 |  | MHz | Standard frequencies: 92.16, 98.304, 100, 122.88, 125, 156.25, 153.6, 163.84, 166.65, 204.8 MHz  |
| Frequency calibration  |  |  | ±1.0 | ppm | Initial accuracy at 25°C ±2°C |
| Reflow shift |  |  | ±1.0 | ppm | Pre to post reflow ∆F (measured ≥ 60 minutes after reflow) |
| Operating temperature range | -40 |  | 85 | °C |  |
| Frequency stability over temperature |  |  | ±0.25 | ppm | Reference to (FMAX + FMIN)/2 |
| Frequency slope |  |  | ±0.1 | ppm/°C | Minimum of 1 frequency reading every 2°C, over the operating temperature range |
| Supply voltage stability |  |  | ±0.1 | ppm | ±5% variation, reference to frequency at 3.3 V |
| Load sensitivity |  |  | ±0.1 | ppm | ±5pF variation, reference to frequency at 5 pF |
| Long term stability (ageing) |  |  | ±1.5±2±4 | ppm | 1 year3 years10 years |
| Acceleration sensitivity |  | 2 |  | ppb/*g* | Gamma vector, 3 axes, 30-1500 Hz |
| Start-up time |  |  | 1 | ms | 90% amplitude |
| Supply voltage (VDD ) |  | 3.32.5 |  | V | ±5%, Fn = 50 – 160 MHz±5%, Fn = 160 – 204.8 MHz |
| Supply current  |  |  | 14 | mA | 5pF//1kΩ, 100MHz |
| Control voltage range  | 0.250.65 |  | 2.252.65 | V | VDD = 2.5 V (Frequency at Vc = 1.25 V)VDD = 3.3 V (Frequency at Vc = 1.65 V) |
| Frequency tuning  | ±5 |  | ±10 | ppm | Frequency shift from min/max to mid Vc |
| Frequency tuning linearity |  |  | 5 | % | Deviation from straight line curve fit |
| Input impedance | 100 |  |  | kΩ |  |
| Oscillator output - CMOSOutput voltage level low (VOL)Output voltage level high (VOH)Rise timeFall timeDuty cycleLoad | 80%45 | 1.21.25 | 20%1.51.55510 | V**dd**V**dd**nsns%pF | With capacitive load of 5 pF, 100M HzWith capacitive load of 5 pF, 100 MHzMeasured 20% to 80% Vdd , 5 pF load, 100 MHzMeasured 80% to 20% Vdd , 5 pF load, 100 MHzMeasured at 50% Vdd trigger level, 100 MHz |

**SSB Phase Noise – 98.304 MHz RHT1490 TCXO (Typical value at 25°C, CMOS output)**

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| RMS Jitter = 165 fs(typ. 12 kHz ~ 20 MHz) |

**Model Outline, Recommended Pad Layout**

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| Pin Connections |
| 1\* | Voltage Control (Vc) or GND |
| 2 | Do not connect |
| 3 | GND |
| 4 | Output |
| 5 | Do not connect |
| 6 | Supply Voltage (Vdd) |
| \* Depending on specifications |

**NOTE:** Outline unit is mm. |

**Test Circuit**

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