RHT1490A

The RHT1490A is a high frequency, low noise TCXO that delivers world class telecommunications grade stability with low RMS phase jitter. This product's frequency output enables lower system jitter, allowing communication system architects to optimise noise budget and performance. With a frequency stability performance of ±0.25 ppm, its CMOS output generates < 200 fs of RMS phase jitter (for a 98.304 MHz device, bandwidth 12 kHz – 20 MHz). The RHT1490A strikes the optimal balance between close-in phase noise and the noise floor, making it suited to be the single reference clock used for both network and air interface requirements. Its ultra-low noise floor performance helps to achieve very low system clock RMS jitter levels needed in high speed interfaces.

Features

- Stability as low as ±0.25 ppm
- Low jitter 200 fs (12 kHz to 20 MHz)
- High frequency from 50 – 204.8 MHz
- Patented "Tilt Compensation" to guarantee performance for life of equipment
- Inherent airflow resistance

Applications

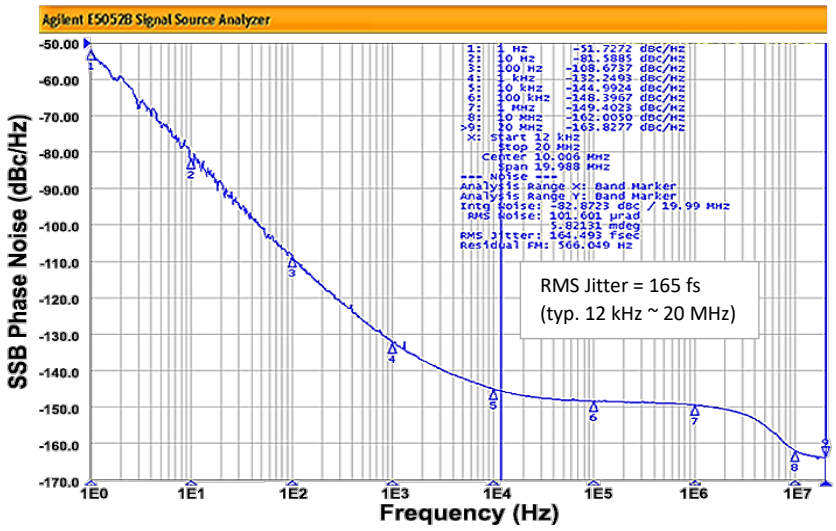
- Sync PLL Embedded Switches
- Designs requiring low noise
- ITU-T G.813 and G.8262
- Low noise C-RAN radios, Microwave links and Small Cells
- Radio head Clock Recovery (IEEE 1588/SyncE)
- 10/25/40G Ethernet

14.4 x 9.2 x 4.7 mm

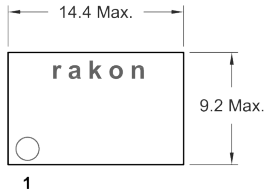
Standard Specifications

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency		50 – 204.8		MHz	Standard frequencies: 92.16, 98.304, 100, 122.88, 125, 156.25, 153.6, 163.84, 166.65, 204.8 MHz
Frequency calibration			±1.0	ppm	Initial accuracy at 25°C ±2°C
Reflow shift			±1.0	ppm	Pre to post reflow ΔF (measured ≥ 60 minutes after reflow)
Operating temperature range	-40		85	°C	
Frequency stability over temperature			±0.25	ppm	Reference to $(F_{MAX} + F_{MIN})/2$
Frequency slope			±0.1	ppm/°C	Minimum of 1 frequency reading every 2°C, over the operating temperature range
Supply voltage stability			±0.1	ppm	±5% variation, reference to frequency at 3.3 V
Load sensitivity			±0.1	ppm	±5pF variation, reference to frequency at 5 pF
Long term stability (ageing)			±1.5 ±2 ±4	ppm	1 year 3 years 10 years
Acceleration sensitivity		2		ppb/*g*	Gamma vector, 3 axes, 30-1500 Hz
Start-up time			1	ms	90% amplitude
Supply voltage (V_{DD})		3.3 2.5		V	±5%, Fn = 50 – 160 MHz ±5%, Fn = 160 – 204.8 MHz
Supply current			14	mA	5pF//1kΩ, 100MHz
Control voltage range	0.25 0.65		2.25 2.65	V	V_{DD} = 2.5 V (Frequency at Vc = 1.25 V) V_{DD} = 3.3 V (Frequency at Vc = 1.65 V)
Frequency tuning	±5		±10	ppm	Frequency shift from min/max to mid Vc
Frequency tuning linearity			5	%	Deviation from straight line curve fit
Input impedance	100			kΩ	
Oscillator output - CMOS					
Output voltage level low (V_{OL})			20%	VDD	With capacitive load of 5 pF, 100M Hz
Output voltage level high (V_{OH})	80%			VDD	With capacitive load of 5 pF, 100 MHz
Rise time		1.2	1.5	ns	Measured 20% to 80% VDD , 5 pF load, 100 MHz
Fall time		1.2	1.5	ns	Measured 80% to 20% VDD , 5 pF load, 100 MHz
Duty cycle	45		55	%	Measured at 50% VDD trigger level, 100 MHz
Load		5	10	pF	

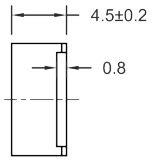
SSB Phase Noise – 98.304 MHz RHT1490 TCXO (Typical value at 25°C, CMOS output)



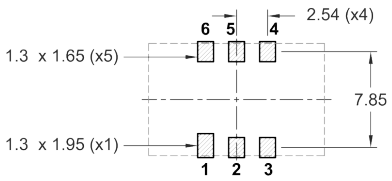
Model Outline, Recommended Pad Layout



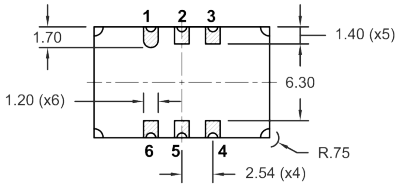
TOP VIEW



SIDE VIEW



RECOMMENDED PAD LAYOUT - TOP VIEW



BOTTOM VIEW

PIN CONNECTIONS

1*	Voltage Control (Vc) or GND
2	Do not connect
3	GND
4	Output
5	Do not connect
6	Supply Voltage (V_{DD})
	* Depending on specifications

NOTE:
Outline unit is mm.

Test Circuit