**RHT1490J**

The RHT1490J is a high frequency Stratum 3 TCXO specifically designed to meet telecommunications grade stabilities at high frequencies with low phase jitter. This product’s frequency output enables lower system jitter, allowing communication system architects to optimise noise budget and performance. Having the optimal balance between close-in phase noise and the noise floor, makes it suitable to be the single reference clock used for both network and air interface requirements. Its ultra-low noise floor performance helps to achieve very low system clock RMS jitter levels need in high speed interfaces (40G/100G).

Comfortably achieving Stratum 3 grade stability, its CMOS output generates < 200 fs of RMS phase jitter (12 kHz – 20 MHz), in a 14 x 9 mm SMD package. An ideal reference clock solution for SyncE and Packet clock requirements (ITU-T G.813, G.8262, G.82673.2 and G8273.3), it also works with both discrete and integrated IEEE 1588 solutions – providing excellent medium term stability for low loop bandwidth applications.

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| Features | Applications  |  | 14.4 x 9.2 x 4.7 mm |
| * Telecommunications grade Stratum 3 stability
* Low jitter < 200 fs (12 kHz to 20 MHz)
* High frequency options from 50 – 200 MHz
* Inherent airflow resistance
 | * Stratum 3 equipment
* Carrier Ethernet/Microwave
* Telecom PLLs
* ITU-T G.813, G.8262, G.82673.2 and G8273.3
* Radio Head Clock Recovery (IEEE 1588/SyncE)
* 10/25/40/100G Ethernet
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**Standard Specifications**

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| Parameter  | Min. | Typ. | Max. | Unit | Test Condition / Description  |
| Nominal frequency |  | 50 – 200 |  | MHz | Standard frequencies: 98.304, 100, 125, and 156.25 MHz  |
| Frequency calibration  |  |  | ±1.0 | ppm | Initial accuracy at 25°C ±2°C |
| Reflow shift |  |  | ±1.0 | ppm | Pre to post reflow ∆F (measured ≥ 60 minutes after reflow) |
| Operating temperature range | -40 |  | 85 | °C |  |
| Frequency stability over temperature |  |  | ± 0.28 | ppm | The default reference for holdover stability, variable temperature is (FMAX + FMIN)/2 |
| Free-run accuracy |  |  | ±4.6 | ppm | Including frequency calibration, temperature, supply voltage & load changes and 20 years ageing |
| Supply voltage stability |  |  | ±0.1 | ppm | ±5% variation, reference to frequency at 3.3 V |
| Load sensitivity |  |  | ±0.1 | ppm | ±5 pF variation, reference to frequency at 5 pF |
| Long term stability (ageing at 40°C) |  |  | ±10±2.5 | ppbppm | Per day, after 10 days of continuous operation20 years |
| Acceleration sensitivity |  | 2 |  | ppb/*g* | Gamma vector, 3 axes, 30 – 1500 Hz |
| Start-up time |  |  | 1 | ms | 90% amplitude |
| Supply voltage (VDD ) |  | 3.32.5 |  | V | ±5%, Fn = 50 – 160 MHz ±5%, Fn = 160 – 200 MHz |
| Supply current  |  |  | 14 | mA | 5 pF//1 kΩ, 100 MHz |
| Oscillator output - CMOSOutput voltage level low (VOL)Output voltage level high (VOH)Rise timeFall timeDuty cycleLoad | 80%45 | 1.21.25 | 20%1.51.555 | V**dd**V**dd**nsns%pF | With capacitive load of 5pF, 100 MHzWith capacitive load of 5pF, 100 MHzMeasured 20% to 80% Vdd , 5 pF load, 100 MHzMeasured 80% to 20% Vdd , 5 pF load, 100 MHzMeasured at 50% Vdd trigger level, 100 MHz |

**SSB Phase Noise – 98.304 MHz RHT1490 TCXO (Typical value at 25°C, CMOS output)**

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| RMS Jitter = 165 fs(typ. 12 kHz ~ 20 MHz) |

**Model Outline, Recommended Pad Layout**

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| Pin Connections |
| 1 | GND |
| 2 | Do not connect |
| 3 | GND |
| 4 | Output |
| 5 | Do not connect |
| 6 | Supply Voltage (Vdd) |

**NOTE:** Outline unit is mm. |

**Test Circuit**

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