RST2016HC

The RST2016HC is a series of high temperature TCXO (Temperature Compensated Crystal Oscillator) and VCTCXO (Voltage Controlled Temperature Compensated Crystal Oscillator) with CMOS output. It is designed for high-performance Automotive and communication applications where the required frequency stability ±2 ppm over operating temperature ranges from -40 to 105°C.

The RST2016H has an analogue ASIC for the oscillator and a high-order temperature compensation circuit in a small font factor 2.0 x 1.6 x 0.7 mm package. This low-power SMD TCXO provides a voltage control option of VCTCXO, with a wide frequency range available from 13 to 52 MHz. Supply voltage options are 1.8 to 3.3 V.

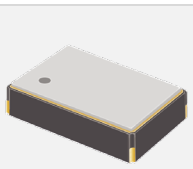
Features

- High-end operating temperature up to 105°C
- Excellent phase noise performance
- Output: CMOS

Applications

- Automotive
- Communications
- Consumer devices
- Wi-Fi

2.0 x 1.6 x 0.7 mm



Standard Specifications

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency (Fn)		13 – 52		MHz	
Frequency calibration			±1	ppm	Offset from nominal frequency measured at 25°C ±2°C
Reflow shift			±1	ppm	Two consecutive reflows
Operating temperature range	-40		105	°C	The operating temperature range over which the frequency stability is measured
Frequency stability over temperature			±2	ppm	Referenced to the midpoint between minimum and maximum frequency value over the specified temperature range[1]
Static temperature hysteresis			0.6	ppm	Frequency change after reciprocal temperature ramped over the operating range. Frequency measured before and after at 25°C
Sensitivity to supply voltage variations			±0.1	ppm	V_{DD} varied ±5% at 25°C
Sensitivity to load variations			±0.1	ppm	±10% load change at 25°C[2]
Long term stability (Ageing)			±1	ppm	Frequency drift over 1 year at 25°C
Supply voltage (V_{DD})		1.8 – 3.3		V	With a tolerance of ±5%
Supply current			3.8	mA	At maximum V_{DD}[2]
Power down	≥80% 		 ≤20%	VDD	Oscillation Enable (VIH) Oscillation Disable (VIL)
Output voltage level low (VOL) Output voltage level high (VOH)	 90		10	%VDD	Measured with a capacitive load of 15pF
Duty cycle	45		55		Measured at 50% VDD trigger level
Output load			15	pF	
Start-up time Normal mode Fast mode			3 2	ms	@ 26 MHz ±2.5 ppm
Rise time / Fall time			5	ns	@ 10% to 90% VDD, CMOS output

[1] Parts should be shielded from drafts causing unexpected thermal gradients. Temperature changes due to ambient air currents on the oscillator can lead to short term frequency drift.

[2] Specified for load stated in oscillator output section at 25°C.

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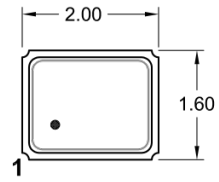
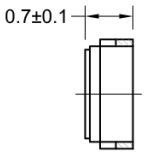
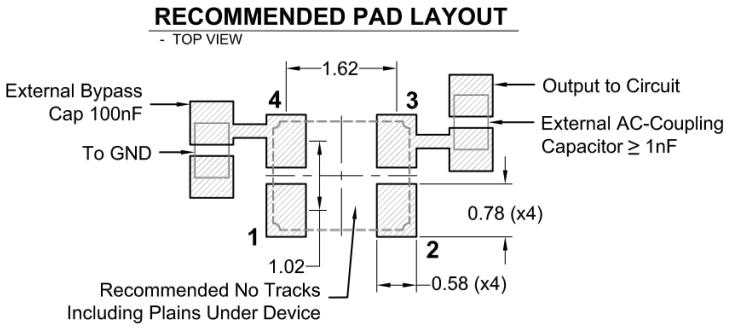
Model Outline and Recommended Pad Layout

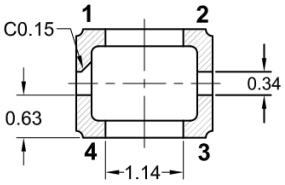


TOP VIEW



SIDE VIEW





BOTTOM VIEW

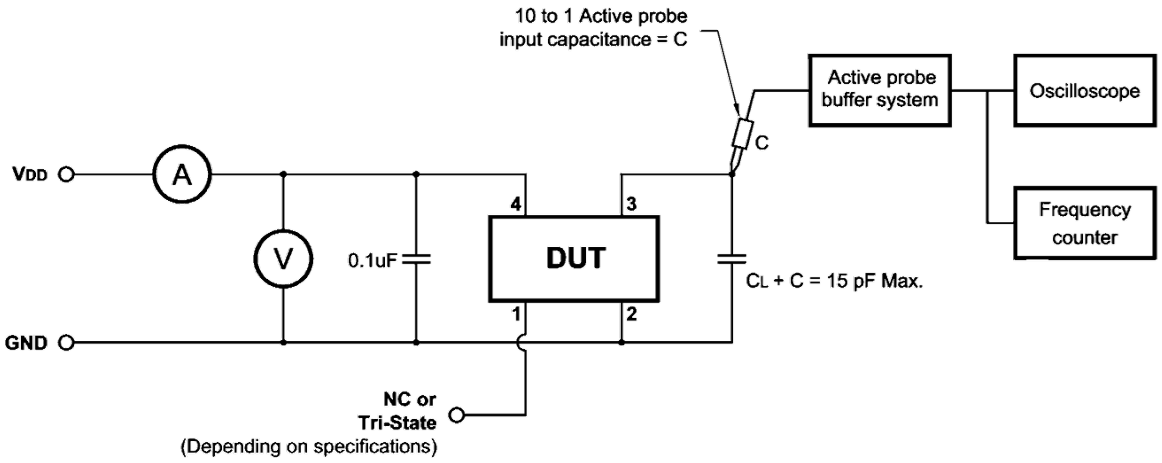
Pin	Connections
1*	NC or Tri-state (see table below)
2	GND
3*	Output (see table below)
4	Supply voltage (V_{DD})

Pin 1	Pin 3
High	Output
Floating	Output
Low	High-Impedance

NOTE: Dimensions are in millimetre.

Test Circuit

CMOS OUTPUT:



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