RK205 5032

This radiation tolerant 5 x 3.2 mm hermetically sealed SMD VCXO is specifically designed for missions where resistance to demanding environment, short lead-time and radiation tolerance are required. It combines a very low RMS phase jitter, tight frequency stability and is available with different types of FM screening options.

Features

- Free from export restrictions
- TID limit of 72/100 kRad and latch-up free till 32.4/62 MeV
- Hermetically sealed package
- Frequency range: 8-1500 MHz
- Low consumption: 30 mA
- Supply voltage: 2.5 or 3.3 V
- AFD[1] ±50 ppm over -40°C to +85°C
- Different screening options

Applications

- Missions where TID limit of 72/100 kRad and latch-up free till 32.4/62 MeV are required
- Rugged environment

5.0 x 3.2 mm

1. Environmental Conditions

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
Operating temperature	Option I: -40°C to 85°C Option M: -55°C to 125°C	-40 -55	25 25	85 125	°C
Switch-on temperature	TS_0	-55		125	°C
Non-operating temperature	TNO_P	-55		125	°C
Mechanical shock	MIL-STD-883, Method 2002 (1500 g, 0.5 ms)				
Humidity	After 48 hours at 85°C ±2°, 85% relative humidity non-condensing				
Temperature cycling	MIL-STD-883, Method 1010.8 (-55°C, +125°C, 1000 cycles)				
Vibration	MIL-STD-883, Method 2007 (20 g, 3 different axis, 4 times)				
Gross and fine leak	MIL-STD-883, Method 1014				
RoHS compliant	Yes				

Radiation:
Products have been tested up to the following levels without any events

	TID (LDR as per ESCC22900)	SEL (MeV/mg/cm²)	SET (MeV/mg/cm²)	SEFI (MeV/mg/cm²)
CMOS	100 kRad	32.4	20	62.5
LVDS	72 kRad	32.4	10	62.5
LVPECL	72 kRad	62.5	10	62.5

2. Frequency Characteristics

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
AFD[1] option	Option I: -40°C to 85°C Option M: -55°C to 125°C			±50 ±75	ppm
Initial frequency accuracy (FVT[2] option)				±15	ppm
Frequency stability over temperature (FVT)	Option I: -40°C to 85°C Option M: -55°C to 125°C			±30 ±50	ppm
Supply voltage stability (FVT)	Over operating temperature			±3	ppm
Load sensitivity (FVT)	Over operating temperature			±5	ppm
Ageing (FVT)	Over 10 years			±15	ppm
Start-up time				10	ms

[1] AFD: Absolute Frequency Drift. It includes initial accuracy + temperature range + supply variation + load variation + ageing over 10 years.
[2] FVT: Frequency Vs. Temperature.

3. Electrical Interface

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
Power supply (V_{DD})	Option 2: 2.5 V Option 3: 3.3 V	2.375 2.97	2.5 3.3	2.625 3.63	V
Stead state input current power	CMOS output: LVDS output LVPECL output		20 23 54		mA

4. Control Voltage (Vc)

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Absolute Pull Range (APR)	±50			ppm	
Total pull range			400	ppm	Frequency shift from minimum to maximum Vc
Control voltage (Vc)	0.3	1.65	3.0	V	
Linearity			15	%	Vc from 0.3 to 3V
Slope					Positive only
Modulation BW	10			kHz	Vc from 0.3 to 3V
Input impedance	1			MΩ	

5. Output Characteristics – CMOS[3]

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
Nominal frequency	CMOS output	8		200	MHz
Output voltage (V_{OL})	15pf load			10% V_{DD}	V
Output voltage (V_{OH})	15pf load	90% V_{DD}			V
Duty cycle	@50% V_{DD}	48		52	%
Rise time / Fall time	90% to 10% Vcc			3	ns
RMS Phase Jitter	Integrated 12 kHz to 20 MHz		0.9	2.5	ps

6. Output Characteristics – LVPECL

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
Nominal frequency	LVPECL output	8		1500	MHz
Output voltage (V_{OL})	50Ω nominal load			V_{DD} – 1.6V	V
Output voltage (V_{OH})	50Ω nominal load	V_{DD} – 1.03V			V
Duty cycle	@ V_{DD} – 1.03V (45 to 55% over 600 MHz)	48		52	%
Rise time / Fall time	80% to 20% Vcc			0.6	ns
RMS Phase Jitter	Integrated 12 kHz to 20 MHz		0.9	2.5	ps

[3] The CMOS output is TTL compatible with the 3.3 V supply voltage.

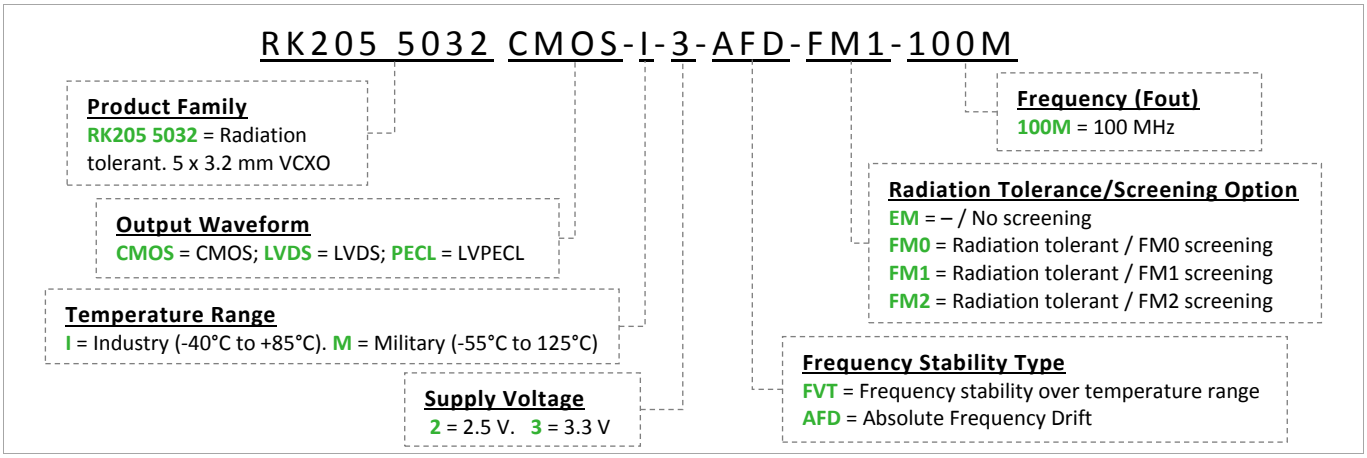
7. Output Characteristics – LVDS

Parameter	Condition / Remarks	Min.	Typ.	Max.	Unit
Nominal frequency	LVDS output	8		1500	MHz
Output voltage	Voltage swing (V_{OD})		350		mV
Duty cycle	Measured @ 1.25 V (45 to 55% over 150 MHz)	48		52	%
Rise time / Fall time	RL = 100 Ω / CL = 10 pF			0.6	ns
RMS Phase Jitter	Integrated 12 kHz to 20 MHz		0.9	2.5	ps

8. Screening Options

Screening Operation	Requirements and Condition	Options			
		EM	FM0	FM1	FM2
Stabilization bake (prior to seal)	MIL-STD-883 method 1008, conduction C	–	24h@150°C	24h@150°C	24h@150°C
Thermal shocks	MIL-STD-883, method 1011, condition A	–	✓	✓	✓
Temperature cycling	MIL-STD-883, method 1010, condition B	–	✓	✓	✓
Constant acceleration	MIL-STD-883, method 1010, condition A Acceleration: 5000g, curing 60s in direction Y1	–	✓	✓	✓
PIND test	MIL-STD-883, method 2020, condition B	✓	✓	✓	✓
Seal test	Fine leak: MIL-STD-883, method 1014, condition A2	✓	✓	✓	✓
	Gross leak: CEI 68-2-17 Test Qc, Method 1	✓	✓	✓	✓
Pre burn-in measurement	Following the guidelines of MIL-PRF-55310, §4.8.5, §4.8.6, §4.8.11, and §4.8.20	✓[4]	✓[5]	✓[5]	✓
Burn-in	Temperature: +125°C Pressure: Patm Supply Voltage: Vcc nom Load: Load nom	–	–	160h min.	160h min.
Post burn-in measurement	Following the guidelines of MIL-PRF-55310	–	–	✓	✓
PDA		–	–	20%	10%
External visual Inspection	MIL-STD-883, Method 2009	–	–	✓	✓

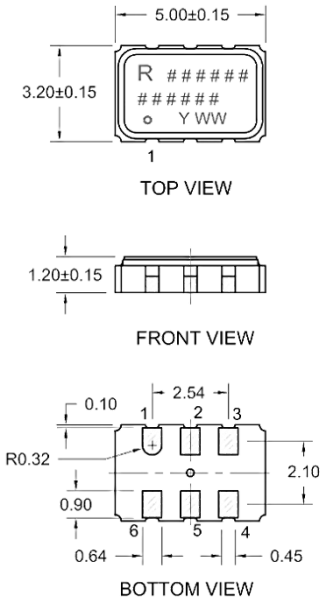
9. Ordering Part Example



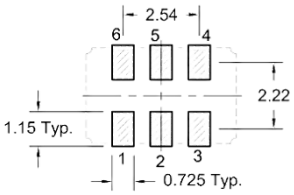
[4] Electrical verification.

[5] MIL-STD-105E general inspection level | AQL level 1.0.
► 100 pcs batch: test on 13 pcs / 0 rejected. ► 500 pcs batch: test on 20 pcs / 0 reject accepted. ► 1000 pcs batch: test on 50 pcs / 1 reject accepted.

10. Model Outline, Pin Connections and Recommended Pad Layout



RECOMMENDED PAD LAYOUT – Top View



NOTE: Outline unit is mm.

PIN CONNECTIONS

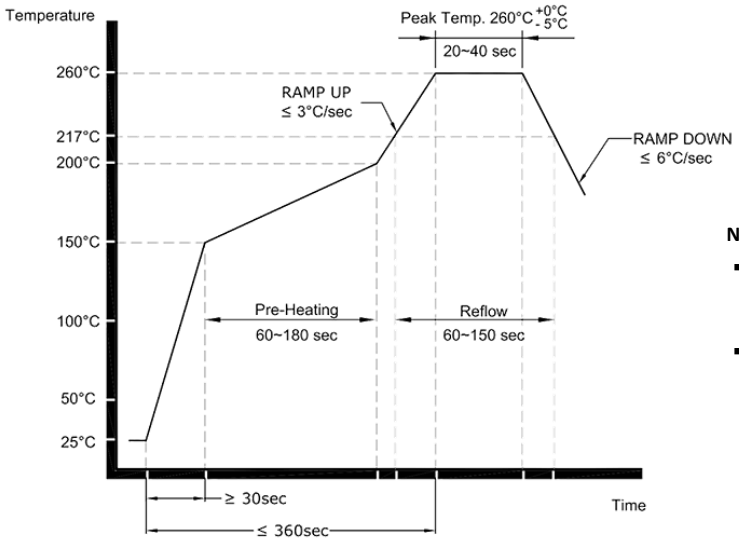
1	Vc
2	E/D* or NC (Not connected, for internal use only)
3	GND (Ground)
4	Fout (Frequency output)
5	Complementary Output (LVPECL/LVDS) or NC
6	VDD (Supply voltage)

* **E** (Output Enable): > 70% of VDD on E/D, or E/D pin left open (Connected to internal pull-up resistor)
D (Output Disable): < 30% of VDD on E/D, or E/D pin to GND

11. Marking

Parameter	Test Condition / Description
Top line	[R ######] R and part identifier
Middle line	[######] Part information
Bottom line	[o YWW] Pin 1, Year code* and Week code** Year code*: A = 2010, B = 2011, C = 2012, D = 2013, … Z = 2035 Week code**: WW = 01 = Week of first Monday of the year

12. Manufacturing Information

Parameter	Test Condition / Description
Packaging description	<300 pcs: Cut-tape >300 pcs: Tape and reel. Standard packing quantity is 2000 units per reel
Pb-free reflow profile	

Note:

- The product has been tested to withstand the Reflow Profile shown on the left hand side.
- The reflow profile used to solder Rakon products is determined by the solder paste manufacture's specification. It is recommended that the reflow profile use does not exceed the one on the left.