

RXO2520C

The RXO2520C is a Crystal Oscillator (XO) in a compact 2.5 x 2.0 mm footprint, designed with a CMOS output for reliable clock generation. Its small form factor makes it an ideal choice for space-constrained Surface-Mount Device (SMD) applications. It delivers ≤ 1 ps RMS phase jitter (measured from a 12 kHz to 20 MHz offset). For applications requiring even lower jitter, an option with typical jitter as low as 50 fs is available upon request.

This device supports a wide range of industry-standard frequencies from 0.5 to 133 MHz. It provides various frequency stability options across a wide operating temperature range, considering factors such as initial frequency calibration, supply and load variations, and one-year ageing effects. The RXO2520C is well-suited for diverse applications in consumer electronics, computing, networking, data centres, industries, and more.

Features

- Frequency (Fn): 0.5 to 133 MHz
- Output: CMOS
- Wide frequency range
- Operating temperature: -40 to 125°C
- Low phase noise and RMS jitter

Applications

- Consumer electronics
- Computing, Networking
- Processing, Data storage
- Data centre
- Medical, Industrial

2.5 x 2.0 mm



Standard Specifications

| Parameter | Min. | Typ. | Max. | Unit | Test Condition / Description |
|------------------------|---|-------------|----------------------|------|---|
| Nominal frequency (Fn) | 0.5 | | 133 | MHz | |
| Temperature range | -40 | | 85 ~ 125 | °C | |
| Frequency stability | | | $\pm 25 \sim \pm 50$ | ppm | Including frequency calibration, operating temperature range, supply and load variations, and 1 year ageing at 25°C |
| Supply voltage (VDD) | | 1.8/2.5/3.3 | | V | With a tolerance of $\pm 5\%$ |
| Supply current | ≤ 20 MHz ≤ 40 MHz ≤ 60 MHz ≤ 133 MHz | | 6 7 9 18 | mA | |
| RMS phase jitter | | | 1 | ps | Integrated from 12kHz to 20MHz |

Model Outline and Recommended Pad Layout

RECOMMENDED PAD LAYOUT
– TOP VIEW

NOTE:

- All dimensions are in millimetres (mm).
- Model height options are 0.9mm max. or 0.95mm max.

| Pin | Connections |
|-----|----------------------|
| 1* | Enable/Disable (E/D) |
| 2 | GND |
| 3 | Output |
| 4 | VDD |

* Output Enabled: $>70\%$ of VDD on E/D, or E/D pin left open (Connected to internal pull-up resistor)
Output Disabled: $<30\%$ of VDD on E/D, or E/D pin to GND