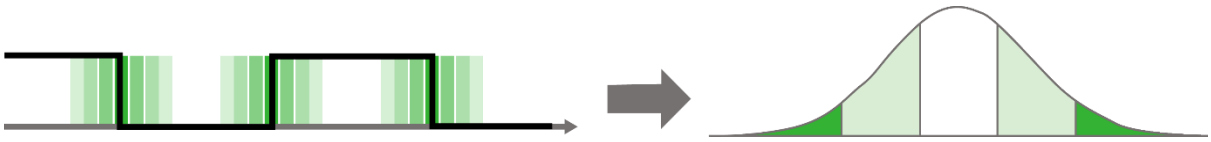
1 Packet Synchronisation and Oscillator Requirements

1.1 Introduction

In traditional transport networks, synchronisation information was primarily embedded in the physical layer or in the payloads. Clocks extracted data from physical layer devices (PHYs) or from smoothing the gapped clocks generated from the pay load. The rise of packet based technologies however, has imposed challenges to synchronisation. Ethernet has become the ubiquitous communication platform for computer networks in the home and enterprise. The simplicity, performance and cost effectiveness of Ethernet technology, has made it a viable choice for transport networks as well. There are challenges with adapting Ethernet technology for carrier class highly reliable, managed networks. The inherently asynchronous Ethernet has the primary challenge of carrying time sensitive traffic, like real time voice or video data.

1.2 Stationary and Non Stationary Significant Events

Traditional synchronisation is based on physical layer technologies and works in a master/slave configuration. In order to recover the clock from the master end, the slave captures significant events from the master and filters them to remove any variation that may have occurred from the master to slave propagation. In traditional synchronisation, the significant events are the clock transitions that happen at the slave end which are received from the master. When the probability distribution of these significant events is analysed, a stationary behaviour of the signal is observed with a defined mean and variance.



Stationary signals can be filtered with defined loop bandwidths and the desired results of noise removal can be achieved.

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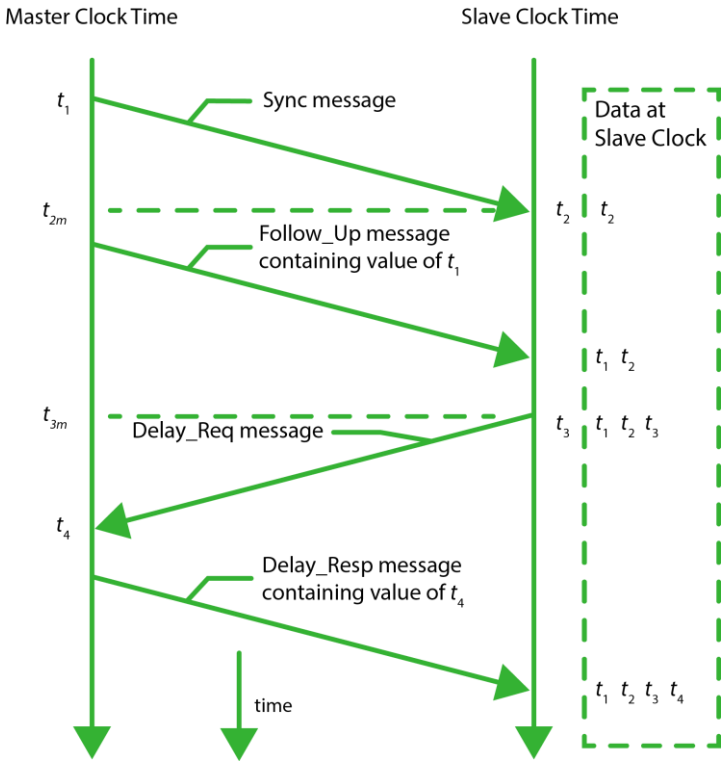
In packet networks, time stamps are significant events. They are inherently statistical in nature and the characteristics of their probability distributions also change with time. This is primarily due to the statistical multiplexing of packets in the intermediate nodes, when propagating from a master element to a slave element.

The following example shows a histogram of packet delays which is essentially derived from the arrival time stamps. The example shows varying load on a 10-switch network and corresponding variation in the histograms. There could be other variables, including the following: the number of nodes from master to slave, the synchronisation packet rates, the mix of load packet sizes (QoS) related to the queuing and shaping of the switching/routing elements and so on.



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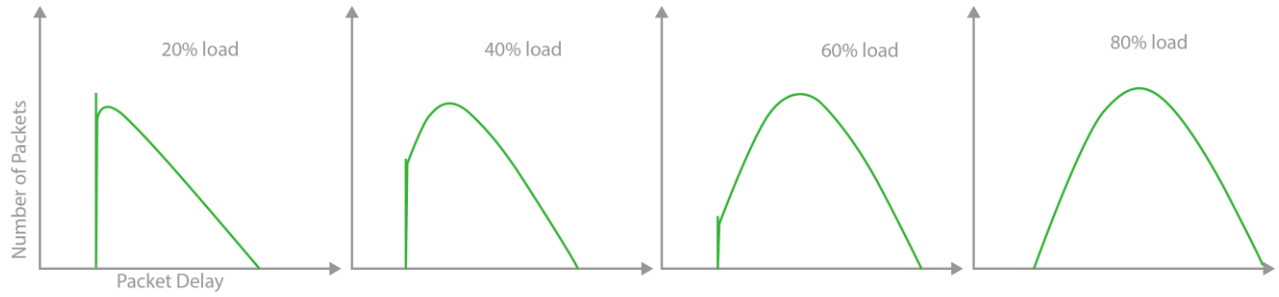

1.3 Packet Filtering and Long Time Constant Filters

The network interface timing performance requirements of the packet network clocks must be in line with the interface timing requirements of the traditional networks, in order to ensure interoperability and co-existence of the two types of equipment in the network. In order for a system to meet the interface timing requirements, a minimum number of timing packets need to be available at the synchronisation slave. This applies over a specific packet delay range and time window for the timing recovery process. These requirements are referred to as Floor Packet Percentiles in G.8260. In order to address the issue of widely varying packet delays, ITU-T suggests the use of a packet selection block in the packet based clock functional model in the ITU – T G.8263 recommendation. The standard also suggests having second order Phase Locked Loop (PLL) implementations with suggested loop filter values such as 1mHz which indicates time constants in the order of thousands of seconds.

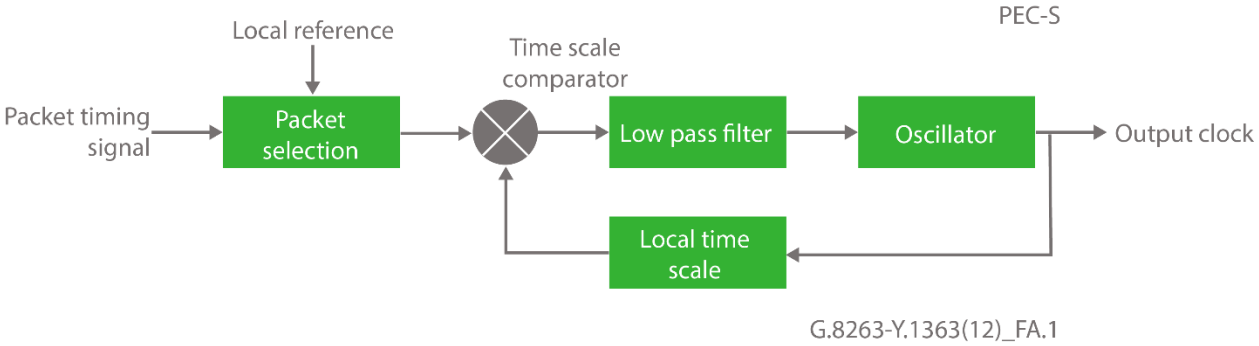

Figure A – Functional model of a packet-based equipment clock – slave – frequency (PEC-S-F)

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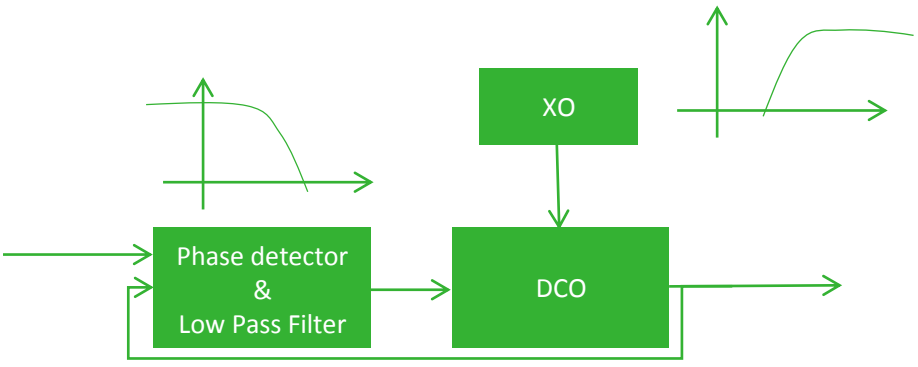
1.4 Synchronisation Loops and Oscillator requirements

There are two general methods of implementing synchronisation loops, either by using a voltage controlled oscillator driven by the filtered phase errors or by using a fixed frequency oscillator and using a Digitally Controlled Oscillator (DCO) to synthesise the variation in the loop. Implementation using a DCO is illustrated in the diagram that follows.



As seen in the diagram, the low pass filter of the synchronisation loop implementation removes the noise from the network. At the same time an equivalent cut-off frequency generating high-pass filtered oscillator noise, is presented to the system. This means the noise is dependent on the loop bandwidth of the Phase Locked Loop (PLL), which is a compromise between the network noise and the oscillator noise. As the loop bandwidth of the PLL is narrowed to filter out the network noise, the oscillator's capability of noise generation within the limits defined by the standards becomes important.

Defining the oscillator solution requires knowledge of the difference in frequency versus the temperature. Full characterisation is determined by defining the temperature ramp and measurement rate and completing a detailed analysis over the characterisation time period.

There are many different approaches to design an oscillator meeting the technical requirements; each offer trade-offs in relation to performance, size, reliability and cost. Rakon is able to advise the best oscillator solution by combining its understanding of the application requirements with expertise in a wide range of oscillator technologies including resonator design, IC development, packaging, testing and manufacturing. Rakon has already characterised various types of oscillators under changing environmental conditions for the loop time periods, relevant to standards' requirements.

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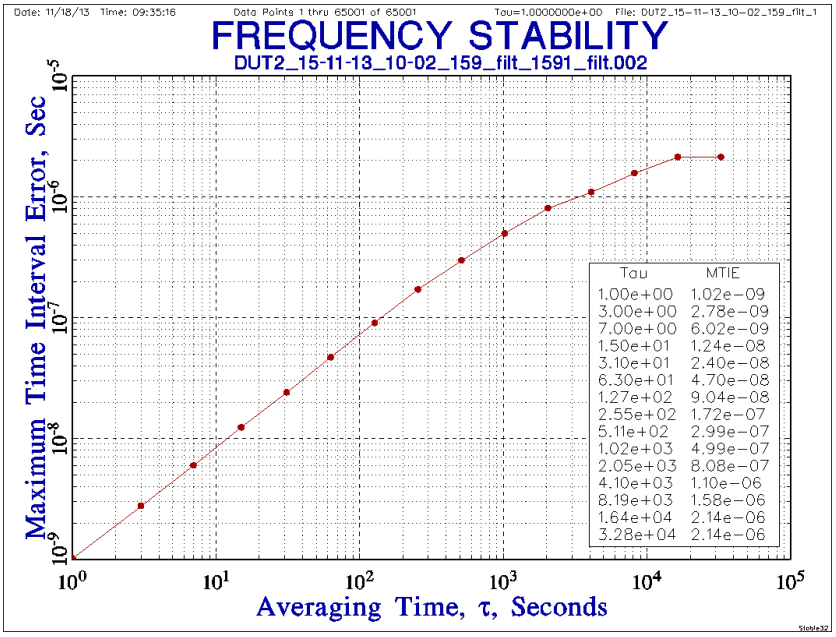
1.5 Time Constants and Temperature Effects on Oscillators

With a 1mHz bandwidth (usually related to Stratum 3E clocks) on a first order loop implementation, the time constant can be assumed to be about 160 seconds, assuming a 1/2pi()f relationship. Relating this to a 0.5˚C/min variation, the temperature change that can happen at that time constant is about 1.9˚C. When the loop bandwidths extend to a few thousands seconds, such as for example at 0.05mHz, the time constants are about 3200 seconds. Relating this to a 0.5˚C/min variation the temperature change is about 27˚C. The maximum temperature change possible with a second order loop filter implementation will be very wide as the time constants will be much longer.

At these temperature windows and rates, the frequency performance of the oscillator determines the fit of the oscillator for the application requirement. The performance of the oscillator, filtered with the right loop bandwidth should meet the performance requirements suggested by standards bodies. One such key requirement is the G.8263 Wander generation by ITU-T.

The following MTIE graph shows performance of Mercury devices with 0.1mHz second order loop bandwidth filter applied with a temperature variation of -40/85˚C.



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1.6 Standards Requirements

Network Time Protocol (NTP) and Precision Time Protocol (PTP), (IEEE 1588) define the protocols required to do packet synchronisation; their mechanisms assure interoperability between various nodes supporting the protocol. These include the packet formats, message types, flow details and so on. The IEEE 1588 protocol can be used across various segments and applications and defines "Profiles" to support and select relevant attributes for the specific segment or application. ITU defines the performance aspects of the system, from a telecom perspective. The International Telecommunication Union (ITU) also defines the architecture of networks and network and equipment limits for the packet networks. The G.826x and G.827x family of ITU – T standards define the various standards for synchronisation over packet networks.

The G.8263 and G.8273.x documents define the requirements for the synchronisation performance of equipment clocks, for when they are tested for perfect inputs or defined input impairments.

Rakon oscillators are defined to meet the requirements of these standards.

1.7 Rakon Oscillators for Packet Networks

Rakon offers a wide range of oscillators for packet networks including Temperature Compensated Crystal Oscillators (TCXOs) mini IC-based Oven Controlled Crystal Oscillators (OCXOs) and traditional discrete OCXOs. The following table details the range of Rakon oscillators available for packet networks and outlines the features of each product.

	Pluto™ TCXO (RFPT Series)	Pluto+™ TCXO (RPT Series)	Mercury™ OCXO (ROM Series)	Discrete OCXO (ROX1490 Series)	Discrete OCXO (ROX2522 Series)
FvsT	±100 ppb	±50 ppb	±10 ppb	±10 ppb	±5 ppb
Aging	20 ppb/day	20 ppb/day	1 ppb/day	1 ppb/day	0.5 ppb/day
Slope	20 ppb/°C	15 ppb/°C	1 ppb/°C	0.2 ppb/°C	0.1 ppb/°C
Bandwidth Supported	50 mHz	50 mHz	1 mHz	0.1 mHz	0.05 mHz
Frequency Holdover (250 ppb)	1 week	1 week	>1 month	>3 months	>6 months

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	Pluto ™ TCXO (RFPT Series)	Pluto+™ TCXO (RPT Series)	Mercury ™ OCXO (ROM Series)	Discrete OCXO (ROX1490 Series)	Discrete OCXO (ROX2522 Series)
Time Holdover ±1.5µs @20°C window, 1°C/hour variation	-	-	1 hour	3 hours	4 hours
Power	20 mW	20 mW	350 mW	550 mW	1.5 W
Package Size (mm)	7x5, 5x3.2	7x5, 5x3.2	14x9, 9x7	14x9	25x22
Price	$	$	$$	$$$	$$$$

Rakon oscillator references are available for off-the shelf algorithm vendors supporting IEEE 1588 solutions. Please contact Rakon for more information on the solutions available.

Along with standard compliant solutions for packet networks, Rakon also provides clocking solutions such as crystals, clock oscillators, multi frequency oscillators, Voltage Controlled Crystal Oscillators (VCXOs) and standard TCXOs.

Additional Rakon products for complete Packet Network Synchronisation design

Products Family	Product Series	Key Capabilities
TCXO	High Stability	10 – 52 MHz, ±0.5 – 5 ppm over -40 – 85°C and in 3.2 x 2.5, 2.5 x 2.0 or 2.0 x 1.6 mm packages.
VCXO	M / P / R	10 to 460 MHz with low phase-noise and CMOS/PECL/LVDS in 7.0 x 5.0 mm or 5.0 x 3.2 mm packages.
XO	S	With different dual or quad frequency outputs at the same time: from 10 to 460 MHz. CMOS/PECL/LVDS/HCSL output types available.
	M / P / R	10 to 460 MHz with <1 ps jitter and CMOS/PECL/LVDS/HCSL in 7.0 x 5.0, 5.0 x 3.2 or 2.5 x 2.0 mm packages.
	X / Z	1 to 50 MHz commercial CMOS output in 1.6 x 1.2, 2.0 x 1.6, 2.5 x 2.0 or 3.2 x 2.5 mm packages.
Crystals	RSX / RTF	RSX: 12 to 48 MHz for ethernet, WiFi and USB. RTF: 32 kHz for real time clocks.

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