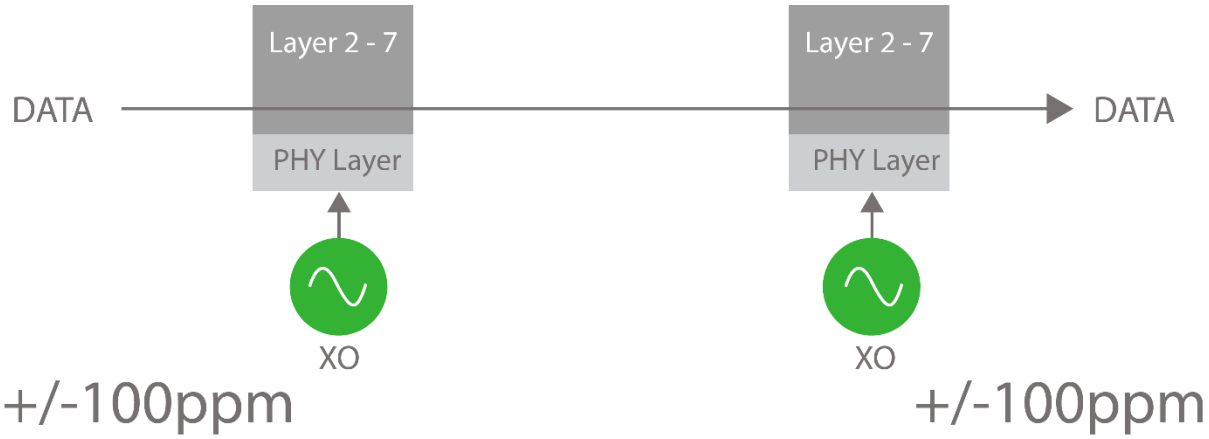
# 1 Oscillators for Synchronous Ethernet Applications

## 1.1 Introduction

Ethernet is the ubiquitous communication platform for computer networking in the home and enterprise. The simplicity, performance and cost effectiveness has made Ethernet technology a viable choice for transport networks as well. There are challenges in adapting Ethernet technology to carrier class, highly reliable managed networks. The inherently asynchronous nature of Ethernet has the primary challenge of carrying time sensitive traffic such as real time voice or video data.

## 1.2 Asynchronous to Synchronous

Traditionally Ethernet nodes were running asynchronously to each other, with a defined maximum ±100ppm deviation from nominal frequency. Most of the traffic carried over Ethernet was asynchronous and 'bursty' in nature. For example, the email and internet Internet Protocol (IP) packet traffic, carried over the Ethernet is bursty in nature in the sense that it is usually grouped in large chunks and transmitted over irregular intervals. Synchronisation in its strict sense was not required because of the nature of the traffic going through. Transceiver buffers were used to take care of the unexpected variations in the data flow. Moreover, at the protocol layer, the buffer level triggers from the hardware sent software control messages to "Pause" and "Flow Control" frames transmitted from the source.



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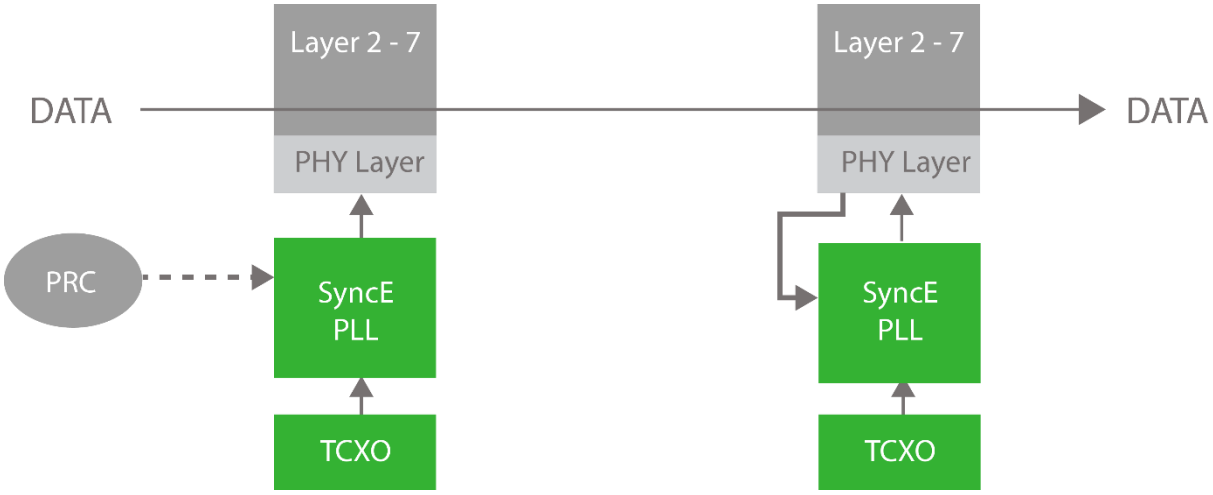
As Ethernet started to carry real time voice and video data, the traffic patterns changed. Such services demanded Constant Bit Rate (CBR) or Variable Bit Rate (VBR) with the contiguous traffic. Such patterns demanded all nodes in a network (from source to destination) to have the same average frequency. The timing and synchronisation techniques that were applied to the traditional circuit switched networks became relevant to the Ethernet networks as well. To enable the Ethernet to carry mobile network backhaul traffic, it is required to have synchronisation supported. The network-equipment, based on Ethernet networks that support synchronous timing are described as Synchronous Ethernet (SyncE) networks.

## 1.3 Synchronised Clocks at the Physical Layer

Ethernet physical layer devices (PHYs) convert the transmitted logic signals to line-coded signals with an embedded local clock and then format them as balanced signals for transmission over copper or fibre cables. At the receiver end, the clock data recovery mechanism of the PHY recovers the signals, and then decodes and convert them to logic levels. The extracted clock output from the PHY is 'cleaned up' to generate the system clock and is then propagated downstream on the network.



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## 1.4 Standards Requirements

ITU-T has formed standards for Ethernet networks that are equivalent to the synchronous transport networks. The Recommendation ITU-T G.8010/Y.1306 (2004), describes the *Architecture of Ethernet layer networks*. The Recommendation ITU-T G.8262/Y.1362, defines the *Timing characteristics of a synchronous Ethernet equipment slave clock (EEC).* The EEC recommendation defines the minimum requirements for timing devices used in synchronising network equipment that supports synchronous Ethernet. The EEC characteristics define equipment limits for clocks. Clock implementations should comply with standalone and synchronous performance limits and should be tolerant to input clock variations. The standards require the equipment to perform holdover functions and be resistant to impairments to the synchronisation flow.

## 1.5 Rakon Oscillators for Synchronous Ethernet

Typically the EEC system is implemented with a Phase Locked Loop (PLL) filtering the PHY extracted clock. There are many aspects of the performance requirements that are defined in the standard, but from an oscillator perspective, the free-run accuracy, wander generation and holdover are the key parameters. The local oscillator used in the PLL system needs to be compliant to the free running accuracy defined by G.8262. In the event that the system starts off without being able to lock to an incoming reference, the output clock accuracy defaults to the accuracy of the oscillator. This value is defined as ±4.6ppm for G.8262. As the oscillator presents a high pass filter effect in the loop, during wander generation, the time domain performance (MTIE and TDEV) of the oscillator needs to be within the limits defined by G.8262 at 0.1Hz, which is the loop bandwidth defined by Option 2 of the standards. The time domain performance of the oscillator becomes important in this case. When the synchroniser loses reference from the network, it enters a “holdover state” where the system remembers and continues to generate the last known good frequency from the network. The performance of the system is heavily dependent on the oscillator at this stage. The frequency versus temperature performance and the ageing of the oscillator are the influencing factors on the holdover performance of the synchroniser.

The output jitter of the oscillator plays an important role in the system output jitter. The oscillator clock is synthesised by a timing silicon which in turn goes to the transceivers and to the electrical or optical interfaces. The signals go through multiplication, voltage variations, printed circuit board effects and electrical to optical conversions before reaching the output. In chassis based systems, timing and control cards drive backplane clocks and line card PLLs perform clock translation and jitter clean up. In these applications, the output jitter of the system synchroniser may not be very critical. In



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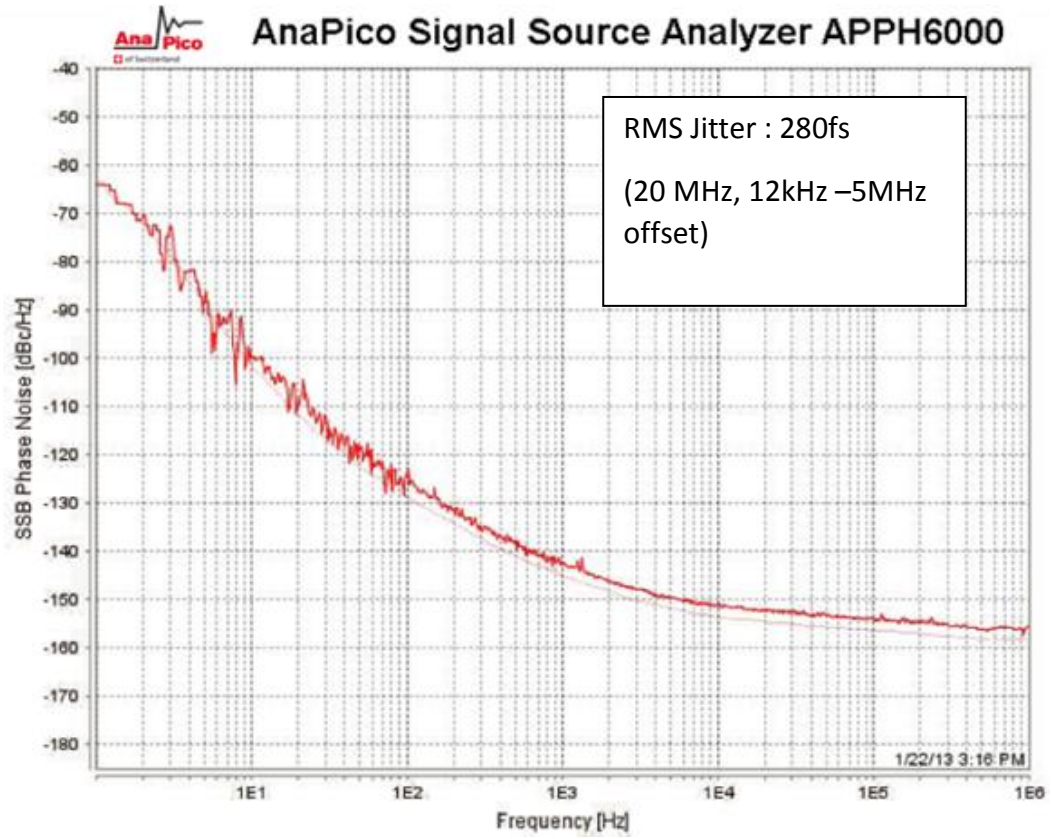
Pizza Box style systems however, the synchroniser clocks will directly drive the transceivers and thus it is critical to have low jitter clocks. Synchronous Ethernet implementations, in general, warrant low jitter timing solutions and the oscillator component of jitter is very important. Rakon's Synchronous

Ethernet solutions provide low jitter clocks to drive interfaces of 10G and beyond, providing the industry with one of the lowest phase noise and rms jitter performance available (in the 12kHz to 5MHz range).

The graph shows an example of jitter performance for a 20MHz device from the 12kHz to 5MHz range.




Rakon provides G.8262 compliant TCXOs for synchronous Ethernet applications. Rakon has qualified oscillators for G.8262 which have undergone extensive time domain performance analysis of the clocks at various frequencies. Rakon has worked with numerous timing and synchronisation silicon



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providers to qualify the solution for complete G.8262 compliance. Please contact Rakon Sales for an approved list of Timing Silicon Vendors and Chipset families. In general, a Stratum 3 level stability oscillator is used for G.8262 compliance applications. However in application scenarios where the system requires higher level of holdover stability or high immunity to temperature effects, higher stability devices like Oven Controlled Crystal Oscillators (OCXOs) are used.

Rakon's Synchronous Ethernet solutions are outlined in the table below:

| Product Family | Product Code | Stability (FvsT) | Jitter @20MHz (12kHz –5MHz) | Package Size (mm) | Standard Compliance |
|---|---|---|---|---|---|
| **TCXO** | RPT7050J | 250 ppb | 290 fs | 7x5 | G.8262, Stratum 3 |
| **IC-OCXO** | ROM9070J, ROM1490J | 50 ppb | 360 fs | 9x7, 14x9 | G.8262, Stratum 3 |
| **IC-OCXO** | ROM1490A, ROM2522A | 50 ppb | 150 fs | 14x9, 25x22 | G.8262, Stratum 3 |
| **OCXO** | ROX1490S4 | 20 ppb | 400 fs | 14x9 | G.8262, Stratum 3E |
| **OCXO** | ROX2522 | 10 ppb | 550 fs | 25x22 | G.8262, Stratum 3E |

Along with the standard compliant solutions for the synchronisation portion of the system, Rakon also provides other clocking solutions including crystals, oscillators, multi frequency oscillators and Voltage Controlled Crystal Oscillators (VCXOs) for other system timing requirements.



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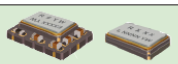
## TCXO Specification

| Parameter | RPT7050P, RPT5032P (Pluto+ TCXO)  | RPT7050N, RPT5032N (Pluto+ TCXO)  |
|---|---|---|
| Package size | 7.0 x 5.0 x **2.0** mm (6 pad)<br>5.0 x 3.2 x 2.1 mm (6 pad)<br>5.0 x 3.2 x 1.65 mm (10 pad) | 7.0 x 5.2 x 2.0 mm (6 pad)<br>5.0 x 3.2 x **2.1 mm (6 pad)**<br>**5.0 x 3.2 x 1.7 mm (4 pad)** |
| Frequency stability over temperature | ±50 ppb (0 to 70°C)<br>±100 ppb (-40 to 85°C) | ±50 ppb (0 to 70°C)<br>±100 ppb (-40 to 85°C) |
| Phase noise | -153 dBc/Hz (20 MHz, 10 kHz offset) | -152 dBc/Hz (20 MHz, 10 kHz offset) |
| Error Vector Magnitude (EMV) | **0.40% typ (3.5 GHz, 100 kHz b/w)** | **0.40% typ (3.5 GHz, 100 kHz b/w)** |
| Holdover over 10 days | ≤ ±100 ppb (0 to 70°C)<br>≤ ±150 ppb (-40 to 85°C) | ≤ ±100 ppb (0 to 70°C)<br>≤ ±150 ppb (-40 to 85°C) |
| Long term frequency stability at 25ºC | ≤ ±10 ppb, 1 day<br>≤ ±100 ppb, 10 days<br>≤ ±1.0 ppm, 1 year<br>≤ ±2.0 ppm, 3 years | ≤ ±10 ppb, 1 day<br>≤ ±100 ppb, 10 days<br>≤ ±1.0 ppm, 1 year<br>≤ ±2.0 ppm, 3 years |

## Additional Rakon products for complete Small Cell design

| Products Family | Product Series | Key Capabilities  |
|---|---|---|
| TCXO | High Stability | 10 – 52 MHz, ±0.5 – 5 ppm over -40 – 85°C and in 3.2 x 2.5, 2.5 x 2.0 or 2.0 x 1.6 mm packages. |
| VCXO | M / P / R | 10 to 460 MHz with low phase-noise and CMOS/PECL/LVDS in 7.0 x 5.0 mm or 5.0 x 3.2 mm packages. |
| XO | S | With different dual or quad frequency outputs at the same time: from 10 to 460 MHz. CMOS/PECL/LVDS/HCSL output types available. |
| | M / P / R | 10 to 460 MHz with <1 ps jitter and CMOS/PECL/LVDS/HCSL in 7.0 x 5.0, 5.0 x 3.2 or 2.5 x 2.0 mm packages. |
| | X / Z | 1 to 50 MHz commercial CMOS output in 1.6 x 1.2, 2.0 x 1.6, 2.5 x 2.0 or 3.2 x 2.5 mm packages. |
| Crystals | RSX / RTF | RSX: 12 to 48 MHz for ethernet, WiFi and USB. RTF: 32 kHz for real time clocks. |



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